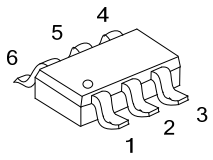
U74AUP1T57

CMOS IC

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



SOT-363

■ DESCRIPTION

The **U74AUP1T57** provides low-power, low-voltage configurable logic gate functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer. All inputs can be connected to V_{CC} or GND.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 2.3V to 3.6V.

The **U74AUP1T57** is designed for logic-level translation applications with input switching levels that accept 1.8 V low-voltage CMOS signals, while operating from either a single 2.5V or 3.3V supply voltage.

The wide V_{CC} range of 2.3V to 3.6V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

■ FEATURES

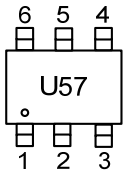
* Low power dissipation
* Wide supply voltage range from 2.3V to 3.6V
* Inputs accept voltages up to 3.6V
* I_{OFF} supports partial-power-down mode

■ ORDERING INFORMATION

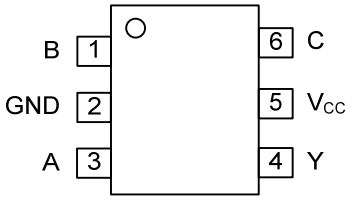
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AUP1T57L-AL6-R	U74AUP1T57G-AL6-R	SOT-363	Tape Reel

U74AUP1T57G-AL6-R
- (1)Packing Type — (1) R: Tape Reel
- (2)Package Type — (2) AL6: SOT-363
- (3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

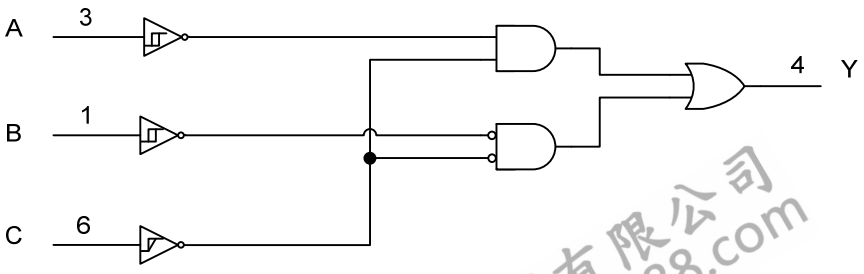
PIN NO.	PIN NAME	I/O	DESCRIPTION
1	B	I	Logic Input 1
2	GND	-	Ground
3	A	I	Logic Input 0
4	Y	O	Logic output
5	V_{CC}	-	Power
6	C	I	Logic Input 2

■ FUNCTION TABLE

INPUT			OUTPUT
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Note: H: High voltage level; L: Low voltage level.

■ LOGIC DIAGRAM (positive logic)



■ FUNCTION SELECTION TABLE

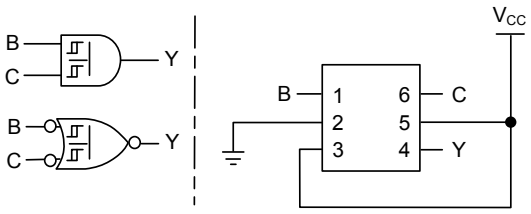


Figure 1. 2-Input AND Gate or 2-Input NOR Gate With Both Inputs Inverted

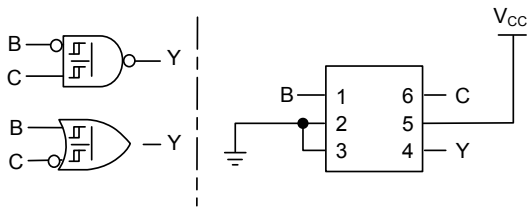


Figure 2. 2-Input NAND Gate With Inverted B Input or 2-Input OR Gate With Inverted C Input

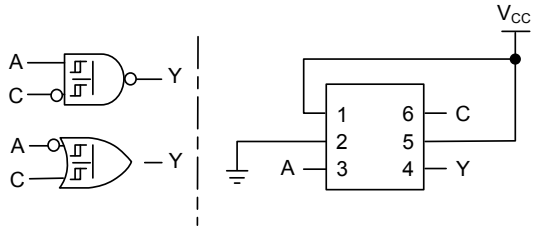


Figure 3. 2-Input NAND Gate With Inverted C Input or 2-Input OR Gate With Inverted A Input

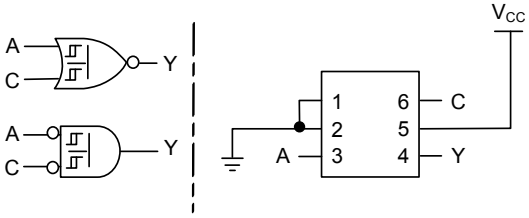


Figure 4. 2-Input NOR Gate or 2-Input AND Gate With Both Inputs Inverted

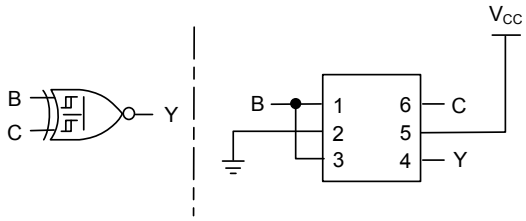


Figure 5. 2-Input XNOR Gate

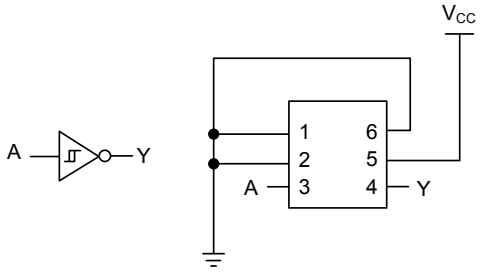


Figure 6. Inverter

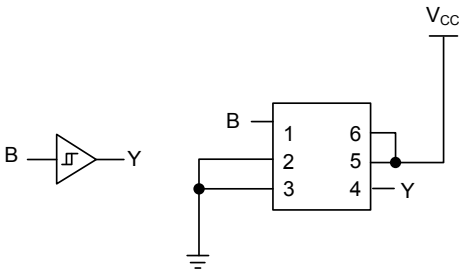


Figure 7. Buffer

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +4.6	V
Input Voltage	V_{IN}		-0.5 ~ +4.6	V
Output Voltage	V_{OUT}	Output in the power-off state	-0.5 ~ +4.6	V
		Output in the high or low state	-0.5 ~ V_{CC}+0.5	V
Continuous V_{CC} or GND Current	I_{CC}		±50	mA
Continuous Output Current	I_{OUT}		±20	mA
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0V	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.6		3.6	V
Input Voltage	V_{IN}		0		3.6	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V_{T+}	V_{CC}=2.3V~2.7V		0.6		1.1	V
		V_{CC}=3.0V~3.6V		0.75		1.16	V
Negative-Going Input Threshold Voltage	V_{T-}	V_{CC}=2.3V~2.7V		0.35		0.6	V
		V_{CC}=3.0V~3.6V		0.5		0.85	V
Hysteresis Voltage (V_{T+}-V_{T-})	$\triangle V_T$	V_{CC}=2.3V~2.7V		0.23		0.6	V
		V_{CC}=3.0V~3.6V		0.25		0.56	V
High-Level Output Voltage	V_{OH}	V_{CC}=2.3~3.6V, I_{OH}=-20μA		V_{CC}-0.1			V
		V_{CC}=2.3V	I_{OH}=-2.3mA	2.05			V
			I_{OH}=-3.1mA	1.9			V
		V_{CC}=3.0V	I_{OH}=-2.7mA	2.72			V
			I_{OH}=-4mA	2.6			V
Low-Level Output Voltage	V_{OL}	V_{CC}=2.3~3.6V, I_{OL}=20μA				0.1	V
		V_{CC}=2.3V	I_{OL}=2.3mA			0.31	V
			I_{OL}=3.1mA			0.44	V
		V_{CC}=3.0V	I_{OL}=2.7mA			0.31	V
			I_{OL}=4mA			0.44	V
Input Leakage Current (All Inputs)	$I_{I(LEAK)}$	V_{CC}=0~3.6V, V_{IN}=3.6V or GND				±0.1	μA
Power OFF Leakage Current	I_{off}	V_{CC}=0V, V_{IN} or V_{OUT}=0~3.6V				±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=2.3~3.6V, V_{IN}=3.6V or GND, I_{OUT}=0A				0.5	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=2.3V~2.7V, One Input at 0.3V or 1.1V, Other Input at 0 or V_{CC}, I_{OUT}=0A				4	μA
		V_{CC}=3V~3.6V, One Input at 0.45V or 1.2V, Other Input at 0 or V_{CC} I_{OUT}=0A				12	μA
Input Capacitance	C_I	V_{CC}=3.3V, V_{IN}=V_{CC} or GND			1.5		pF
Output Capacitance	C_O	V_{CC}=3.3V, V_{OUT}= V_{CC} or GND			3.0		pF

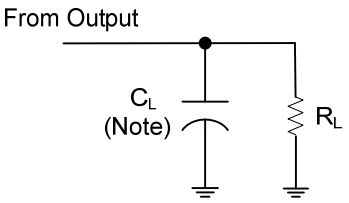
■ SWITCHING CHARACTERISTICS (R_L=1MΩ, T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (A, B or C) to output(Y)	t_{PD}	V_{CC}=2.5V±0.2V V_{IN}=1.8V±0.15V	C_L=5pF	1.8	3.3	5.5	ns
			C_L=10pF	2.3	3.8	6.2	ns
			C_L=15pF	2.6	4.1	6.8	ns
			C_L=30pF	3.8	5.4	8.2	ns
		V_{CC}=2.5V±0.2V V_{IN}=2.5V±0.2V	C_L=5pF	1.7	3.3	5.4	ns
			C_L=10pF	2.1	3.8	6.2	ns
			C_L=15pF	2.5	4.2	6.7	ns
			C_L=30pF	3.3	5.4	8.2	ns
		V_{CC}=2.5V±0.2V V_{IN}=3.3V±0.3V	C_L=5pF	1.4	3.7	4.9	ns
			C_L=10pF	1.8	4.1	5.7	ns
			C_L=15pF	2.2	4.5	6.3	ns
			C_L=30pF	3.0	5.7	7.8	ns
		V_{CC}=3.3V±0.3V V_{IN}=1.8V±0.15V	C_L=5pF	1.6	3.0	3.9	ns
			C_L=10pF	2.0	3.4	4.6	ns
			C_L=15pF	2.3	3.8	5.2	ns
			C_L=30pF	3.4	4.9	6.6	ns
		V_{CC}=3.3V±0.3V V_{IN}=2.5V±0.2V	C_L=5pF	1.6	2.9	4.2	ns
			C_L=10pF	2.0	3.3	4.9	ns
			C_L=15pF	2.3	3.7	5.5	ns
			C_L=30pF	3.1	4.8	6.9	ns
		V_{CC}=3.3V±0.3V V_{IN}=3.3V±0.3V	C_L=5pF	1.3	3.1	4.2	ns
			C_L=10pF	1.7	3.4	4.9	ns
			C_L=15pF	2.0	3.7	5.5	ns
			C_L=30pF	2.8	4.8	7.0	ns

■ OPERATING CHARACTERISTICS (f=10MHz, T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=2.5V		4.0		pF
		V_{CC}=3.3V		5.0		pF

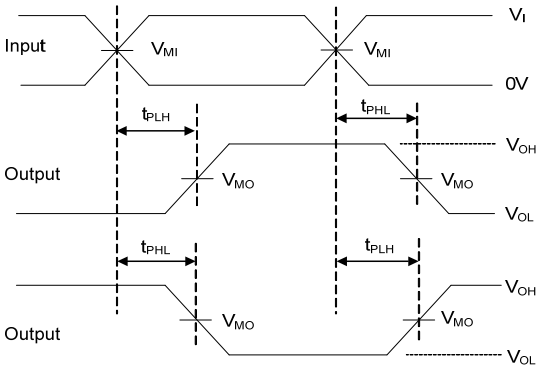
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

Note: C_L includes probe and jig capacitance.

V_{CC}	C_L	V_{MI}	V_{MO}
2.5V±0.2V	5,10,15,30pF	$V_{IN}/2$	$V_{CC}/2$
3.3V±0.3V	5,10,15,30pF	$V_{IN}/2$	$V_{CC}/2$



Voltage Waveforms Propagation Delay Times

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.