



U74CBT1G384

CMOS IC

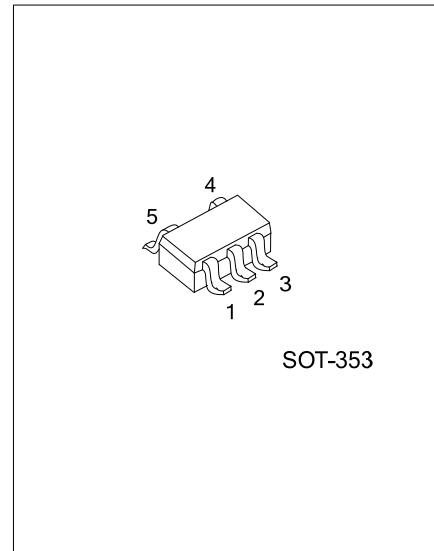
SINGLE FET BUS SWITCH

DESCRIPTION

The **U74CBT1G384** features a single high-speed line switch. The switch is disabled when the output-enable (\overline{OE}) input is high.

FEATURES

- * 5- Ω Switch Connection Between Two Ports
- * Inputs are TTL-Voltage compatible

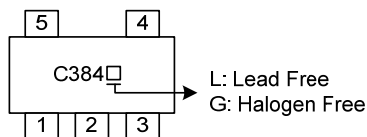


ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBT1G384L-AL5-R	U74CBT1G384G-AL5-R	SOT-353	Tape Reel

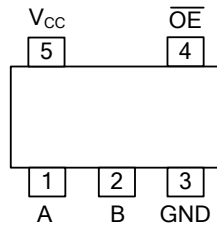
<p>U74CBT1G384G-AL5-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) AL5: SOT-353 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



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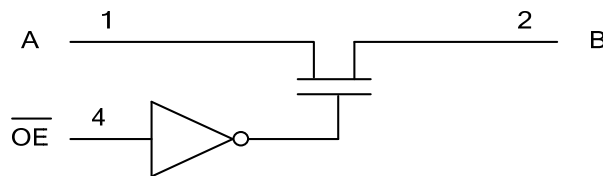
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT \overline{OE}	OUTPUT
L	A port = B port
H	Disconnect

■ LOGIC DIAGRAM (positive logic)



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■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5~7	V
Input Voltage	V _{IN}	-0.5~7	V
Continuous channel current	I _{CH}	128	mA
Input Clamp Current(V _I <0)	I _{IK}	-50	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	4		5.5	V
High-control input voltage	V _{IH}	2			V
Low-control input voltage	V _{IL}			0.8	V
Operating Temperature	T _A	-40		+85	°C

■ STATIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Digital Input Diode Voltage	V _{IK}	V _{CC} =4.5V, I _I =-18mA			-1.2	V	
Input Leakage Current	I _{IN}	V _{CC} =5.5V, V _I =V _{CC} or GND			±1	μA	
V _{CC} or GND Current	I _{CC}	V _{CC} =5.5V, V _I =5.5V or GND, I _O =0			1	μA	
Control input	C _{IN}	V _O =3V or 0		3		pF	
I/O Capacitance (OFF)	C _{IO}	V _O =3V or 0, \overline{OE} = V _{CC}		4		pF	
Resistor between two ports	R _{ON}	V _{CC} = 4V, TYP at V _{CC} = 4V, V _I = 2.4V, I _I = 15mA		14	20	Ω	
		V _{CC} = 4.5V, V _I = 0V	I _I = 64mA		5	7	Ω
			I _I = 30mA		5	7	Ω
		V _{CC} = 4.5V, V _I = 2.4V, I _I = 15mA		10	15	Ω	

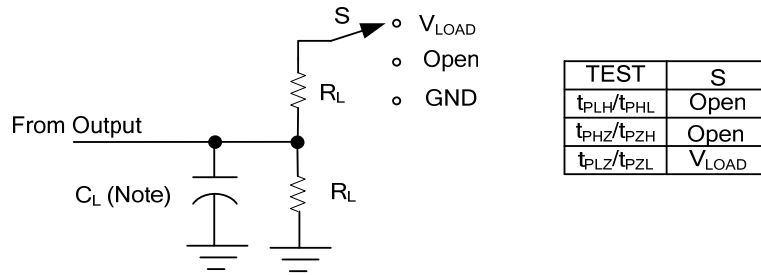
■ DYNAMIC CHARACTERISTICS (Input: t_R, t_F≤2.5ns; PRR≤10MHz; C_L=50pF)

See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A) (Note)	t _{pd}	V _{CC} =4V, C _L =50pF, R _L =500Ω			0.35	ns
		V _{CC} = 5V±0.5V, C _L =50pF, R _L =500Ω			0.25	ns
From input \overline{OE} to output (A or B)	t _{en}	V _{CC} =4V, C _L =50pF, R _L =500Ω			5.5	ns
		V _{CC} = 5V±0.5V, C _L =50pF, R _L =500Ω	1.6		4.9	ns
From input \overline{OE} to output (A or B)	t _{dis}	V _{CC} =4V, C _L =50pF, R _L =500Ω			4.5	ns
		V _{CC} = 5V±0.5V, C _L =50pF, R _L =500Ω	1.0		4.2	ns

Notes: 1. t_{pd}: t_{PLH} and t_{PHL}.
 2. t_{en}: t_{PZL} and t_{PZH}.
 3. t_{dis}: t_{PLZ} and t_{PHZ}.

■ TEST CIRCUIT AND WAVEFORMS ($C_L=50\text{pF}$, $R_L=500\Omega$, $V_{LOAD}=7\text{V}$, $V_M=1.5\text{V}$)



Note: C_L includes probe and jig capacitance.

Fig. 1 Load circuitry for switching times.

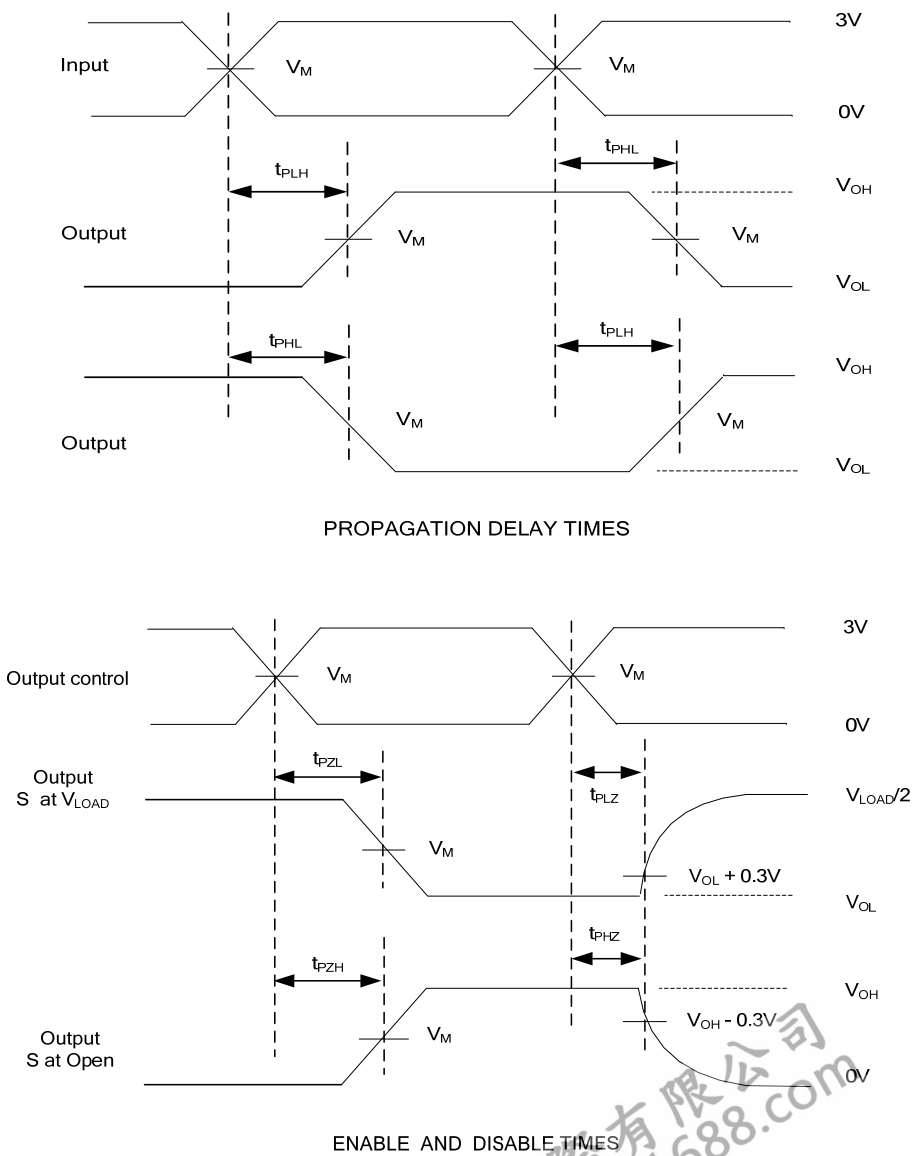


Fig. 2 Propagation delay from input(A) to output(B) and Output transition time.

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