



U74HC00

CMOS IC

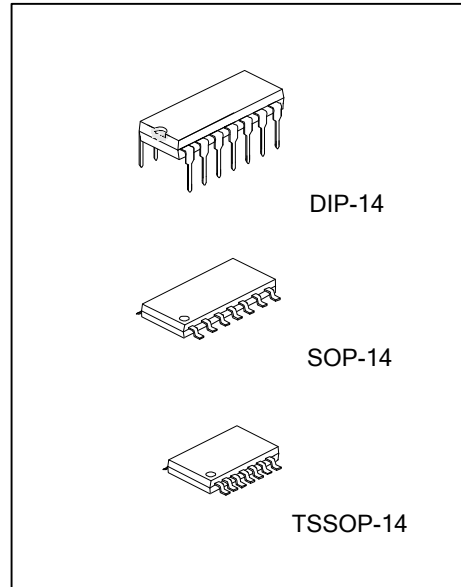
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

DESCRIPTION

The **U74HC00** is a Quadruple 2-input positive-NAND gate with provides the function $Y = A \cdot B$ or $Y = \overline{A + B}$.

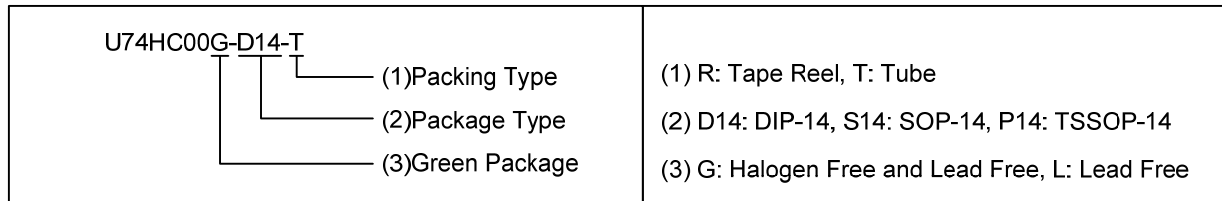
FEATURES

- * Operation voltage range: 2.0 V ~6.0 V
- * Low Quiescent Current: $I_{CC}=2\mu A(\text{Max})$

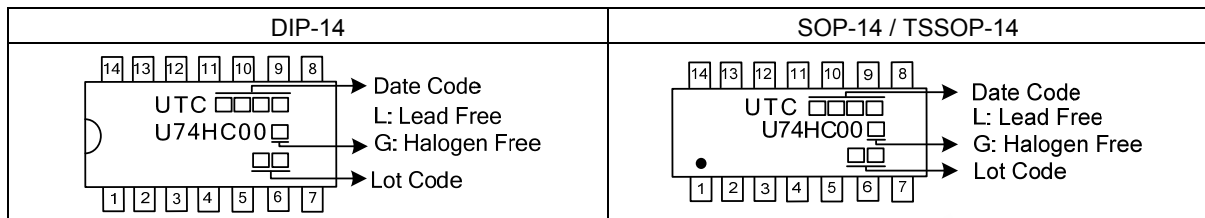


ORDERING INFORMATION

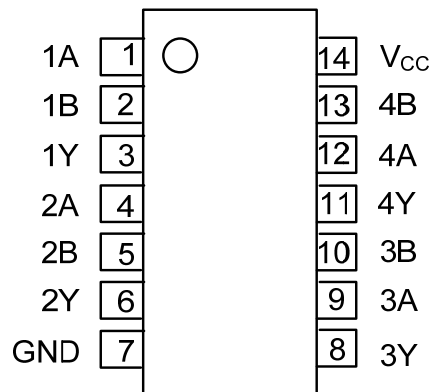
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC00L-D14-T	U74HC00G-D14-T	DIP-14	Tube
U74HC00L-S14-R	U74HC00G-S14-R	SOP-14	Tape Reel
U74HC00L-P14-R	U74HC00G-P14-R	TSSOP-14	Tape Reel



MARKING



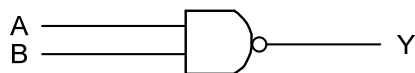
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUT		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

■ LOGIC DIAGRAM (positive logic)



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■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-14	86	°C/W
	DIP-14	80	
	TSSOP-14	113	

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	t_R, t_F	$V_{CC} = 2V$			1000	ns
		$V_{CC} = 4.5V$			500	
		$V_{CC} = 6V$			400	
Operating Temperature	T_A		-40		85	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ STATIC CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC} = 2V$	1.5			V
		$V_{CC} = 4.5V$	3.15			
		$V_{CC} = 6V$	4.2			
Low-Level Input Voltage	V_{IL}	$V_{CC} = 2V$			0.5	V
		$V_{CC} = 4.5V$			1.35	
		$V_{CC} = 6V$			1.8	
High-Level Output Voltage	V_{OH}	$V_{CC} = 2V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -20\mu A$	1.9	1.998		V
		$V_{CC} = 4.5V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -20\mu A$	4.4	4.999		
		$V_{CC} = 6V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -20\mu A$	5.9	5.999		
		$V_{CC} = 4.5V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -4mA$	3.98	4.3		
		$V_{CC} = 6V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -5.2mA$	5.48	5.8		
Low-Level Output Voltage	V_{OL}	$V_{CC} = 2V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OL} = 20\mu A$		0.002	0.1	V
		$V_{CC} = 4.5V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OL} = 20\mu A$		0.001	0.1	
		$V_{CC} = 6V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OL} = 20\mu A$		0.001	0.1	
		$V_{CC} = 4.5V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OL} = 4mA$		0.17	0.26	
		$V_{CC} = 6V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OL} = 5.2mA$		0.15	0.26	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC} = 6V, V_{IN} = V_{CC}$ or 0		±0.1	±100	nA
Quiescent Supply Current	I_Q	$V_{CC} = 6V, V_{IN} = V_{CC}$ or 0, $I_{OUT} = 0$			2	μA
Input Capacitance	C_{IN}	$V_{CC} = 2V \sim 6V$		3	10	pF

■ DYNAMIC CHARACTERISTICS ($T_A=25^\circ\text{C}$, Input: $t_R=t_F=6\text{ns}$; $\text{PRR}\leq 1\text{MHz}$, unless otherwise specified)

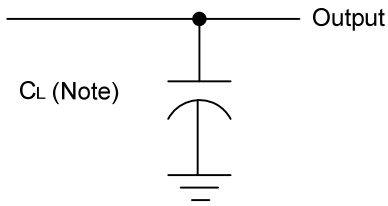
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay, (A) or (B) to (Y)	t_{PLH} , t_{PHL}	$V_{CC}=2\text{V}$, $C_L=50\text{pF}$		45	90	ns
		$V_{CC}=4.5\text{V}$, $C_L=50\text{pF}$		9	18	
		$V_{CC}=6\text{V}$, $C_L=50\text{pF}$		8	15	
Output Transition Times	t_{TLH} , t_{THL}	$V_{CC}=2\text{V}$, $C_L=50\text{pF}$		38	75	ns
		$V_{CC}=4.5\text{V}$, $C_L=50\text{pF}$		8	15	
		$V_{CC}=6\text{V}$, $C_L=50\text{pF}$		6	13	

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

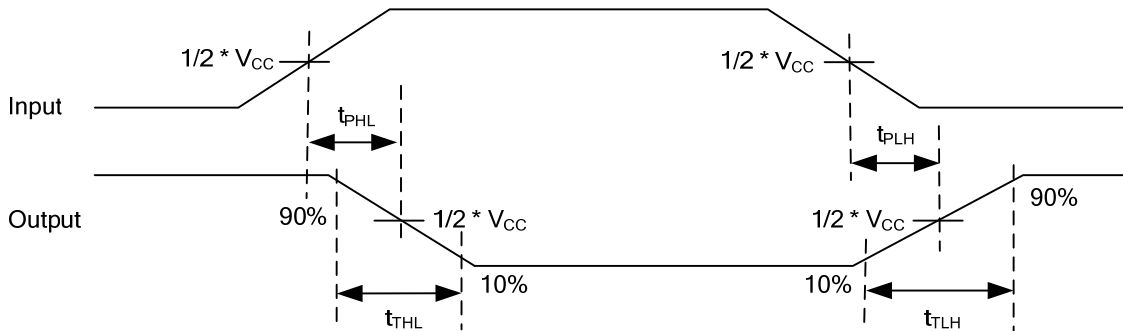
PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Power Dissipation Capacitance	C_{PD}	No Load	20	pF

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ TEST CIRCUIT AND WAVEFORMS



Note: CL includes probe and jig capacitance.



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