

U74HC04

CMOS IC

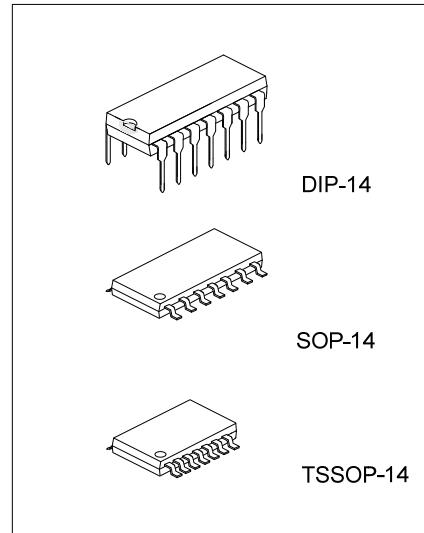
HEX INVERTERS

■ DESCRIPTION

The U74HC04 devices contain six independent inverters.
They perform the Boolean function $Y = \bar{A}$ in positive logic.

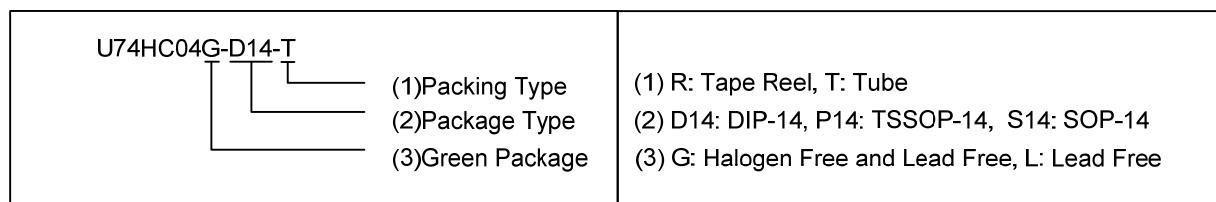
■ FEATURES

- * Wide Operating Voltage Range of 2V to 6V
- * Outputs Can Drive Up To 10 LSTTL Loads
- * Low Power Consumption, 2 μ A Max I_{CC}
- * Typical $t_{pd}=8\text{ns}$
- * $\pm 4\text{mA}$ Output Drive at 5V
- * Low Input Current of 1 μ A Max



■ ORDERING INFORMATION

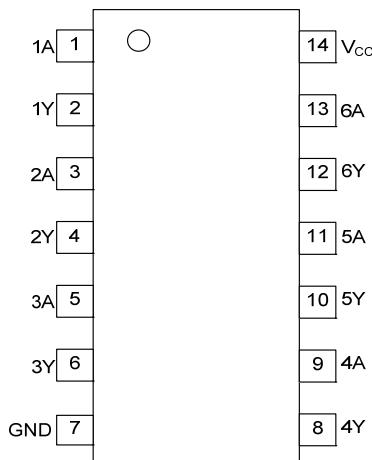
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC04L-D14-T	U74HC04G-D14-T	DIP-14	Tube
U74HC04L-S14-R	U74HC04G-S14-R	SOP-14	Tape Reel
U74HC04L-P14-R	U74HC04G-P14-R	TSSOP-14	Tape Reel



■ MARKING

DIP-14	SOP-14 / TSSOP-14
 Date Code L: Lead Free G: Halogen Free Lot Code	 Date Code L: Lead Free G: Halogen Free Lot Code

■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(Y)
L	H
H	L

■ LOGIC DIAGRAM (positive logic)

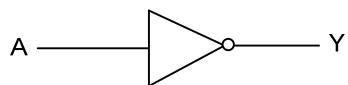


Fig.1 logic diagram for U74HC04

■ ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$, unless otherwise specified) (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Clamp Current($V_I < 0$)	I_{IK}	± 20	mA
Output Clamp Current($V_O < 0$)	I_{OK}	± 20	mA
Output Current	I_{OUT}	± 25	mA
V_{CC} or GND Current	I_{CC}	± 50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-14	80	°C/W
	SOP-14	86	
	TSSOP-14	113	

■ RECOMMENDED OPERATING CONDITIONS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2	5	6	V
Input Voltage	V_I		0		V_{CC}	V
Output Voltage	V_O		0		V_{CC}	V
Operating Temperature	T_A		-40		+85	°C
Input transition rise/fall time	$\Delta t/\Delta V$	$V_{CC} = 2\text{V}$			1000	ns
		$V_{CC} = 4.5\text{V}$			500	
		$V_{CC} = 6\text{V}$			400	

■ STATIC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V_{IH}	$V_{CC} = 2\text{V}$	1.5			V
		$V_{CC} = 4.5\text{V}$	3.15			
		$V_{CC} = 6\text{V}$	4.2			
Negative-Going Input Threshold Voltage	V_{IL}	$V_{CC} = 2\text{V}$		0.5		V
		$V_{CC} = 4.5\text{V}$		1.35		
		$V_{CC} = 6\text{V}$		1.8		
High-Level Output Voltage	V_{OH}	$V_{CC} = 2\text{V}, I_{OH} = -20\mu\text{A}$	1.9	1.998		V
		$V_{CC} = 4.5\text{V}, I_{OH} = -20\mu\text{A}$	4.4	4.499		V
		$V_{CC} = 6\text{V}, I_{OH} = -20\mu\text{A}$	5.9	5.999		V
		$V_{CC} = 4.5\text{V}, I_{OH} = -4\text{mA}$	3.98	4.3		V
		$V_{CC} = 6\text{V}, I_{OH} = -5.2\text{mA}$	5.48	5.8		V
Low-Level Output Voltage	V_{OL}	$V_{CC} = 2\text{V}, I_{OL} = 20\mu\text{A}$		0.002	0.1	V
		$V_{CC} = 4.5\text{V}, I_{OL} = 20\mu\text{A}$		0.001	0.1	V
		$V_{CC} = 6\text{V}, I_{OL} = 20\mu\text{A}$		0.001	0.1	V
		$V_{CC} = 4.5\text{V}, I_{OL} = 4\text{mA}$		0.17	0.26	V
		$V_{CC} = 6\text{V}, I_{OL} = 5.2\text{mA}$		0.15	0.26	V
Input Leakage Current	I_I	$V_{CC} = 6\text{V}, V_I = V_{CC}$ or GND	± 0.1	± 100	nA	
Quiescent Supply Current	I_{CC}	$V_{CC} = 6\text{V}, V_I = V_{CC}$ or GND $I_O = 0$			2	µA
Input Capacitance	C_I	$V_{CC} = 2\text{V}$ to 6V		3	10	pF

■ DYNAMIC CHARACTERISTICS (Input: t_R , $t_F=6\text{ns}$, $C_L=50\text{pF}$; PRR $\leq 1\text{MHz}$)

See Fig. 2 and Fig. 3 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH}/t_{PHL}	$V_{CC}=2\text{V}$		45	95	ns
		$V_{CC}=4.5\text{V}$		9	19	ns
		$V_{CC}=6\text{V}$		8	16	ns
Rise/fall time for output(Y)	t_t	$V_{CC}=2\text{V}$		38	75	ns
		$V_{CC}=4.5\text{V}$		8	15	ns
		$V_{CC}=6\text{V}$		6	13	ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No Load		20		pF

■ TEST CIRCUIT AND WAVEFORMS

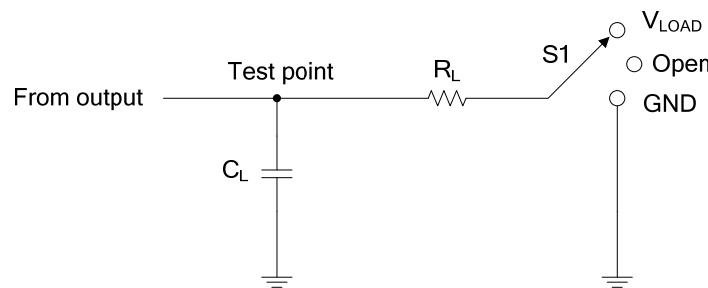
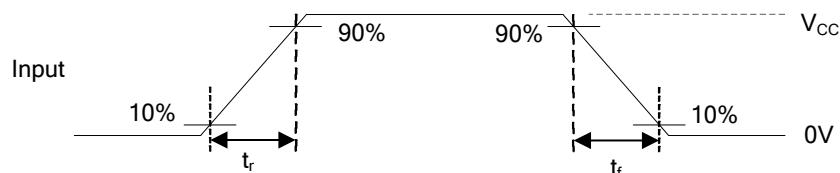
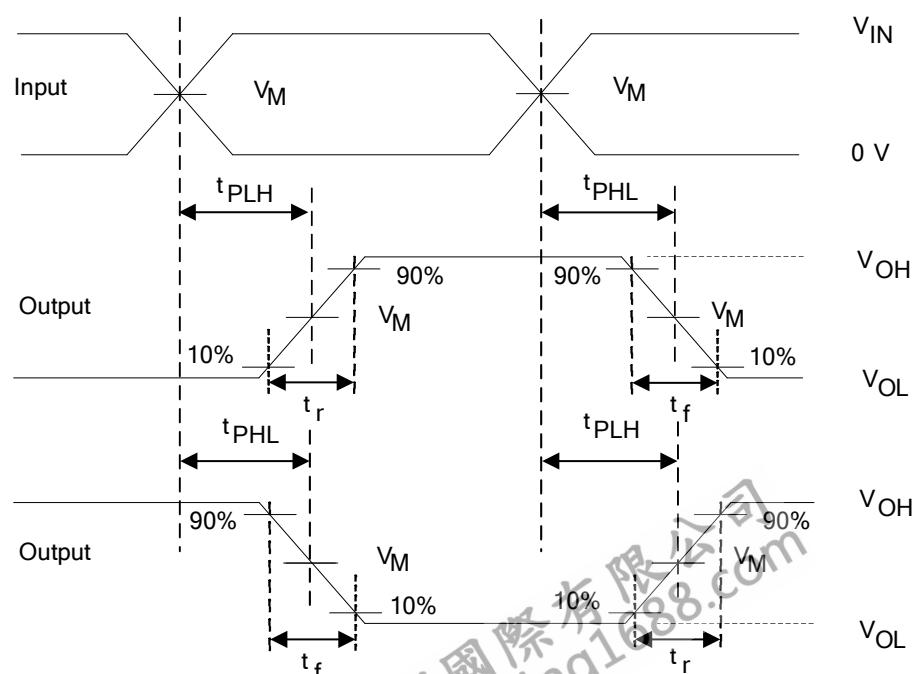


Fig. 2 TEST CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open

Inputs		V_M	V_{LOAD}	C_L
V_{IN}	t_r, t_f	V_M	V_{LOAD}	C_L
V_{CC}	6 ns	$V_{CC}/2$	V_{CC}	50 pF

VOLTAGE WAVEFORMS
INPUT RISE AND FALL TIMESFig.3 VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

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