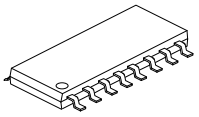
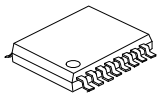
U74HC123

CMOS IC

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET



SOP-16



TSSOP-16

■ DESCRIPTION

The **U74HC123** is high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL).

The U74HC123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}$ =LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering.

An internal connection from $n\overline{R}_D$ to the input gates makes it possible to trigger the circuit by a positive-going signal at input $n\overline{R}_D$ as shown in the function table. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

■ FEATURES

* DC triggered from active HIGH or active LOW inputs
* Retriggerable for very long pulses up to 100% duty factor
* Direct reset terminates output pulse
* Schmitt-trigger action on all inputs except for the reset input

■ ORDERING INFORMATION

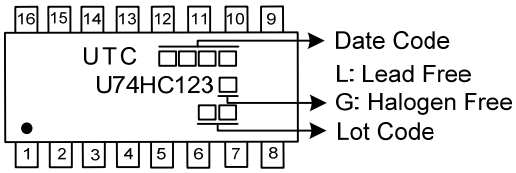
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC123L-S16-R	U74HC123G-S16-R	SOP-16	Tape Reel
U74HC123L-P16-R	U74HC123G-P16-R	TSSOP-16	Tape Reel

U74HC123G-S16-R

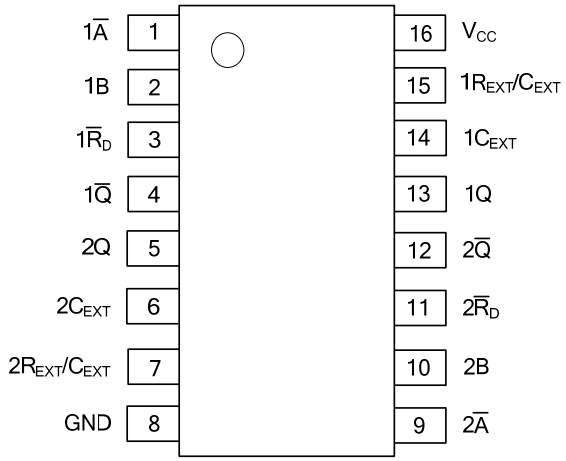
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S16: SOP-16, P16: TSSOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

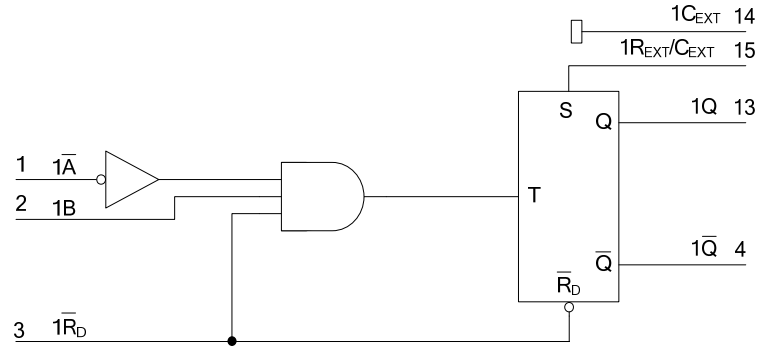


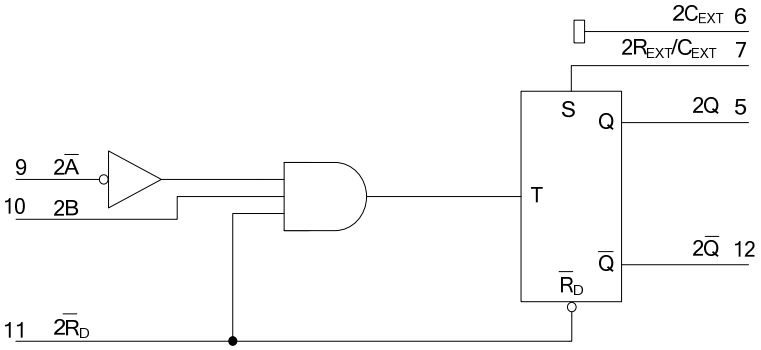
■ FUNCTION TABLE

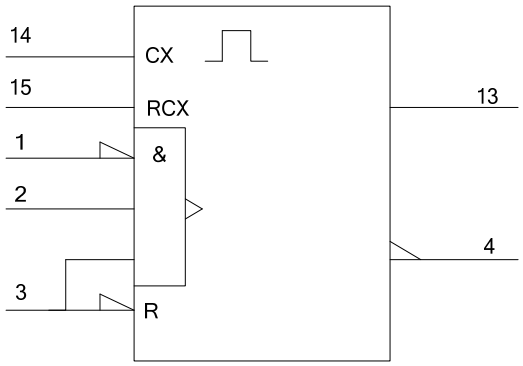
INPUTS			OUTPUTS	
n$\overline{R}_D$	n$\overline{A}$	nB	nQ	n$\overline{Q}$
L	X	X	L	H
X	H	X	L(2)	H(2)
X	X	L	L(2)	H(2)
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

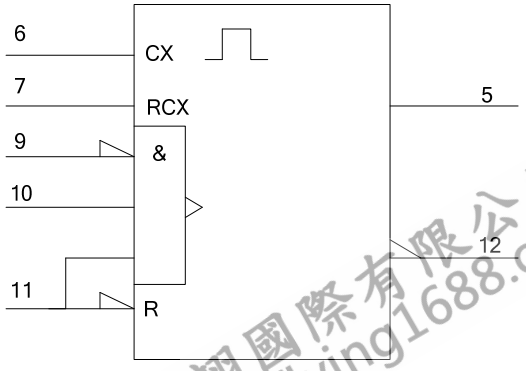
Notes: 1. H: HIGH voltage level L: LOW voltage level X: don'care ↑: LOW-to-HIGH transition
↓: HIGH-to-LOW transition ⎍: one HIGH level output pulse ⎎: one LOW level output pulse
2. If the monostable was triggered before this condition was established, the pulse will continue as programmed.

■ LOGIC SYMBOL



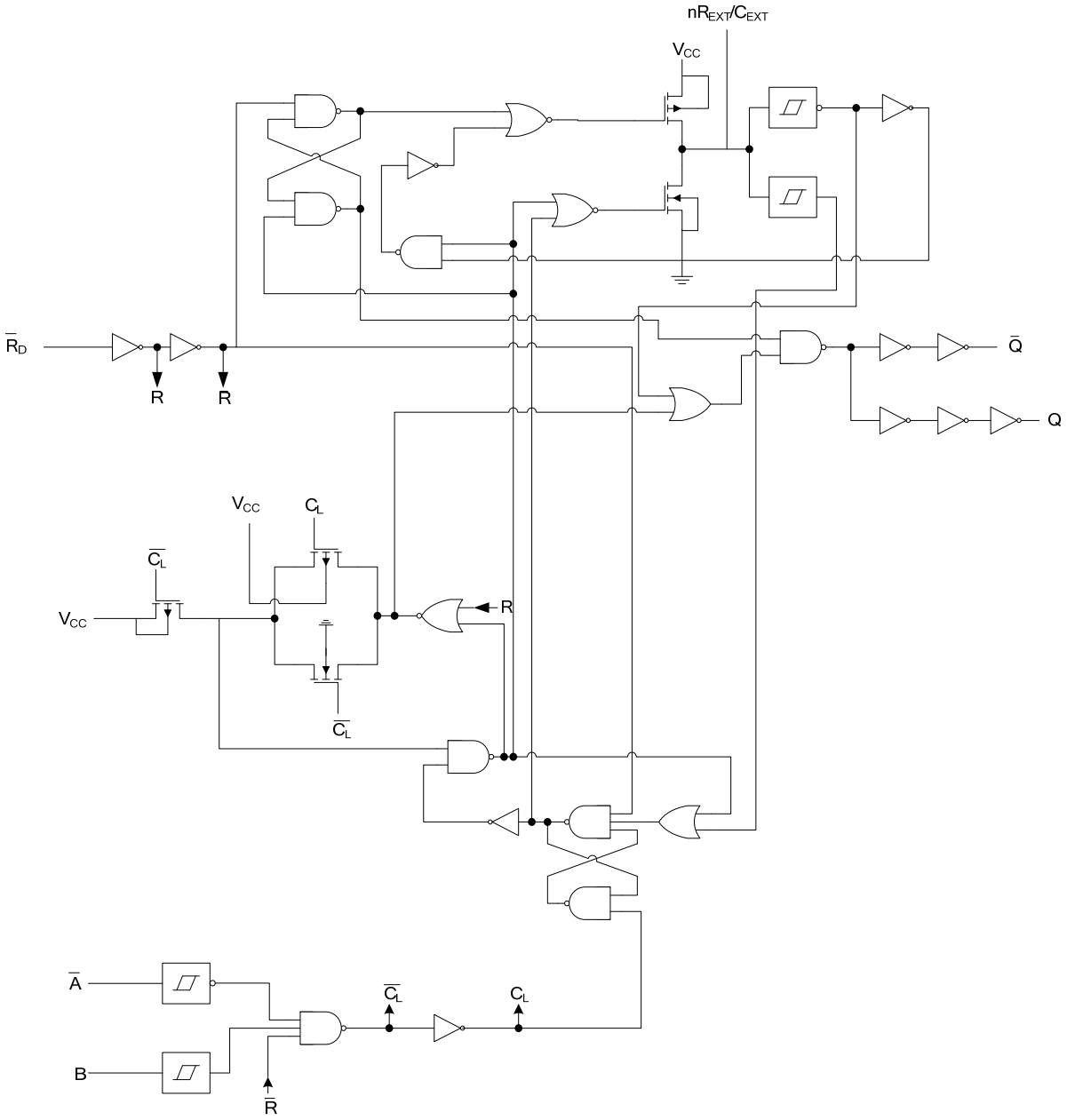






IEC logic symbol

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
V_{CC} or GND Current	I_{CC}	±50	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
High-level Input Voltage	V_{IH}	V_{CC}=2V	1.5	1.2		V
		V_{CC}=4.5V	3.15	2.4		
		V_{CC}=6V	4.2	3.2		
Low-level Input Voltage	V_{IL}	V_{CC}=2V		0.8	0.5	V
		V_{CC}=4.5V		2.1	1.35	
		V_{CC}=6V		2.8	1.8	
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise and Fall Rate $n\overline{R}_D$ Input	△t/△V	V_{CC}=2V			1000	ns
		V_{CC}=4.5V			500	
		V_{CC}=6V			400	
Ambient Temperature	T_{amb}		-40	+25	+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	2		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.5		
		V_{CC}=6V, I_{OH}=-20μA	5.9	6		
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.32		
		V_{CC}=6V, I_{OH}=-5.2mA	5.48	5.81		
Output Voltage Low-Level	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0	0.1	
		V_{CC}=6V, I_{OL}=20μA		0	0.1	
		V_{CC}=4.5V, I_{OL}=4mA		0.15	0.26	
		V_{CC}=6V, I_{OL}=5.2mA		0.16	0.26	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}= V_{CC} or GND			±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8	μA
Input Capacitance	C_I			3.5		pF

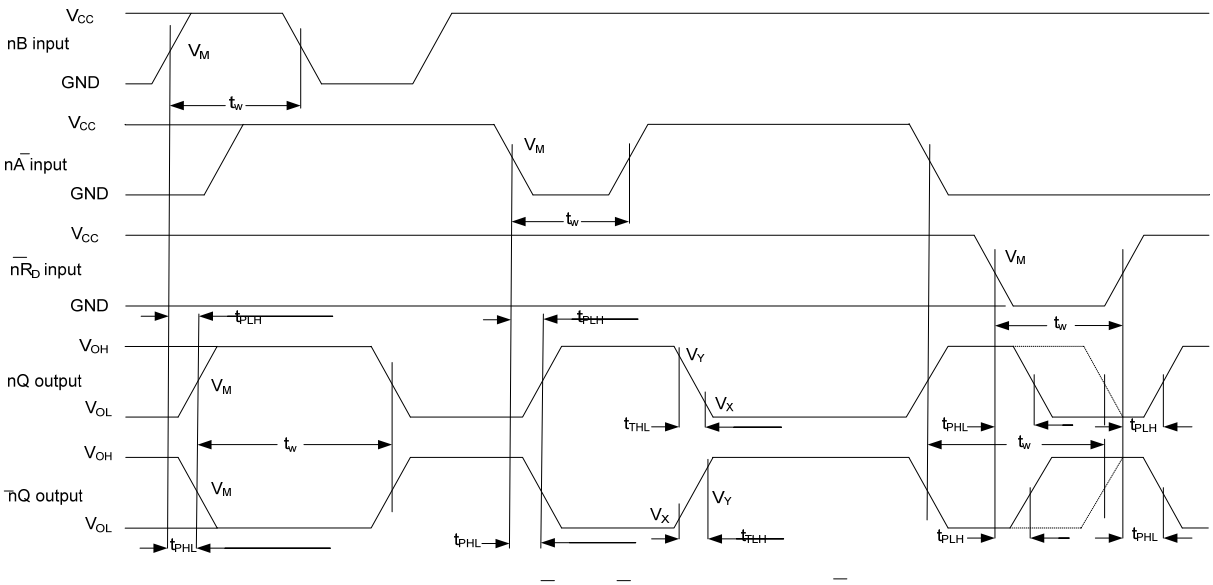
■ SWITCHING CHARACTERISTICS ($t_r = t_f = 6ns$, C_L=50pF, T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay Time From $n\overline{A}$, nB to nQ or $n\overline{Q}$	t_{PLH}/t_{PHL}	V_{CC}=2V	C_{EXT}=0pF R_{EXT}=5k		83	255	ns
		V_{CC}=4.5V			30	51	
		V_{CC}=5V, C_L=15p			26		
		V_{CC}=6V			24	43	
Propagation Delay Time From $n\overline{R}_D$ to nQ or $n\overline{Q}$	t_{PLH}/t_{PHL}	V_{CC}=2V	C_{EXT}=0pF R_{EXT}=5k		66	215	ns
		V_{CC}=4.5V			24	43	
		V_{CC}=5V, C_L=15p			20		
		V_{CC}=6V			19	37	
Output transition time	t_t	V_{CC}=2V			19	75	ns
		V_{CC}=4.5V			7	15	
		V_{CC}=6V			6	13	
Trigger pulse width $n\overline{A}$=LOW	t_w	V_{CC}=2V		100	8		ns
		V_{CC}=4.5V		20	3		
		V_{CC}=6V		17	2		
Trigger pulse width nB=HIGH	t_w	V_{CC}=2V		100	17		ns
		V_{CC}=4.5V		20	6		
		V_{CC}=6V		17	5		
Reset pulse width $n\overline{R}_D$=LOW	t_w	V_{CC}=2V		100	14		ns
		V_{CC}=4.5V		20	5		
		V_{CC}=6V		17	4		
Output pulse width nQ=HIGH, $n\overline{Q}$=LOW	t_w	V_{CC}=5V , C_{EXT}=100nF, R_{EXT}=10k			450		μs
Output pulse width nQ=HIGH, $n\overline{Q}$=LOW	t_w	V_{CC}=5V , C_{EXT}=0pF, R_{EXT}=5k			75		ns
Retrigger time $n\overline{A}$, nB	t_{rt}	V_{CC}=5V , C_{EXT}=0pF, R_{EXT}=5k			110		ns
External timing resistor	R_{EXT}	V_{CC}=2V		10		1000	kΩ
		V_{CC}=5V		2		1000	
External timing capacitor	C_{EXT}	V_{CC}=5V		2		10000	pF

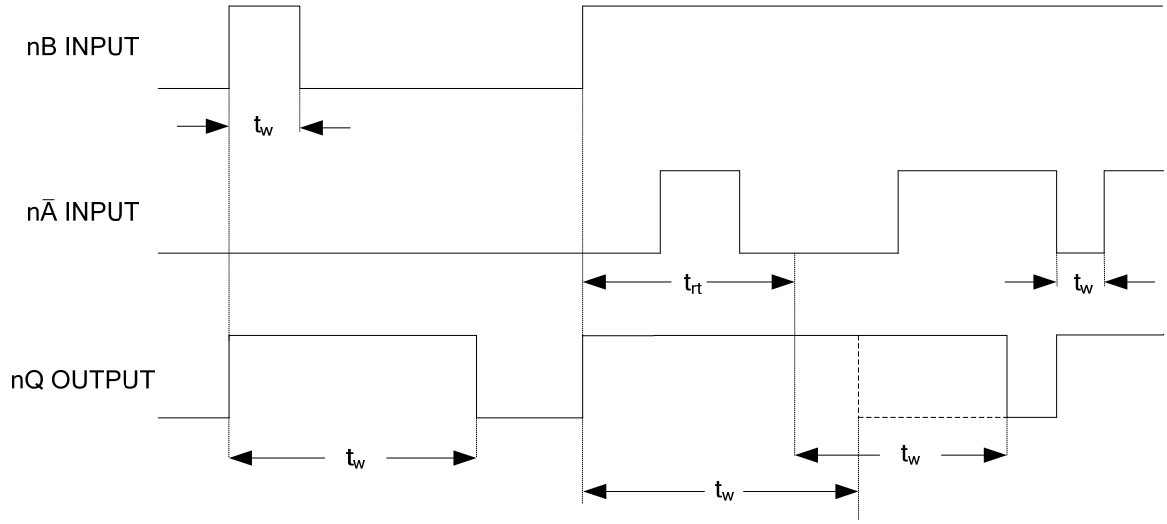
■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance Per monostable	C_{PD}			54		pF

■ TEST CIRCUIT AND WAVEFORMS

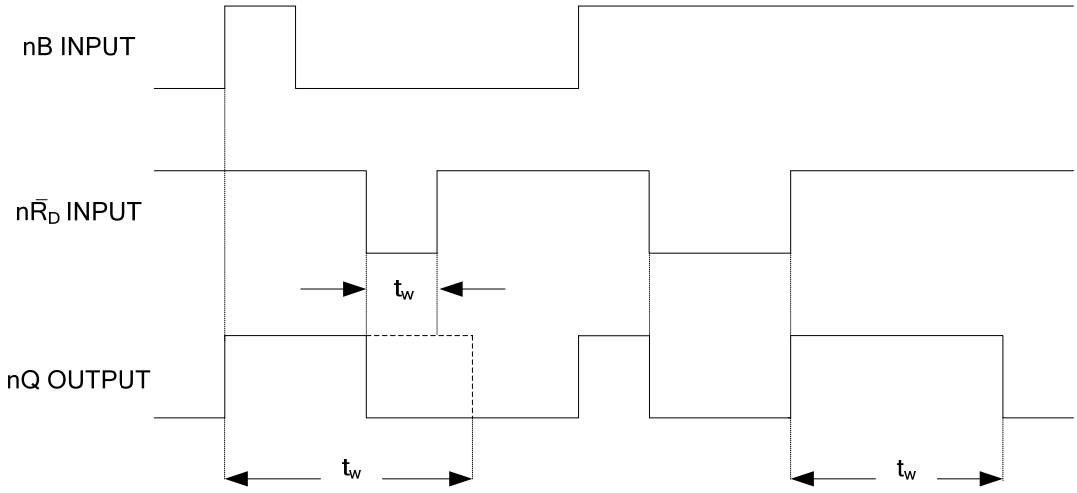


Propagation delays from inputs (nA, nB nR_D) to outputs (nQ, nQ) and output transition times

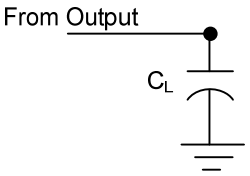


Output pulse control using retrigger pulse; nR_D=HIGH

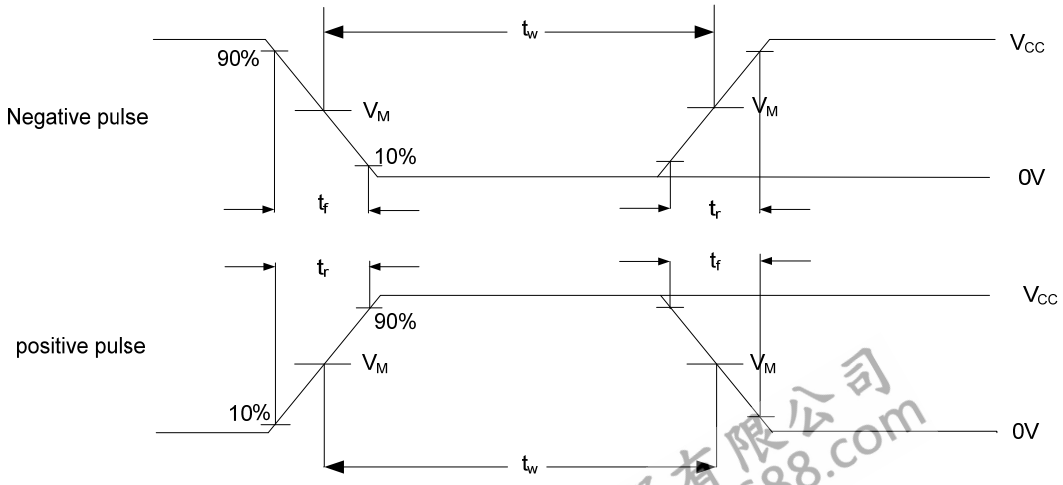
■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Output pulse control using input in nR̄D; nA=LOW



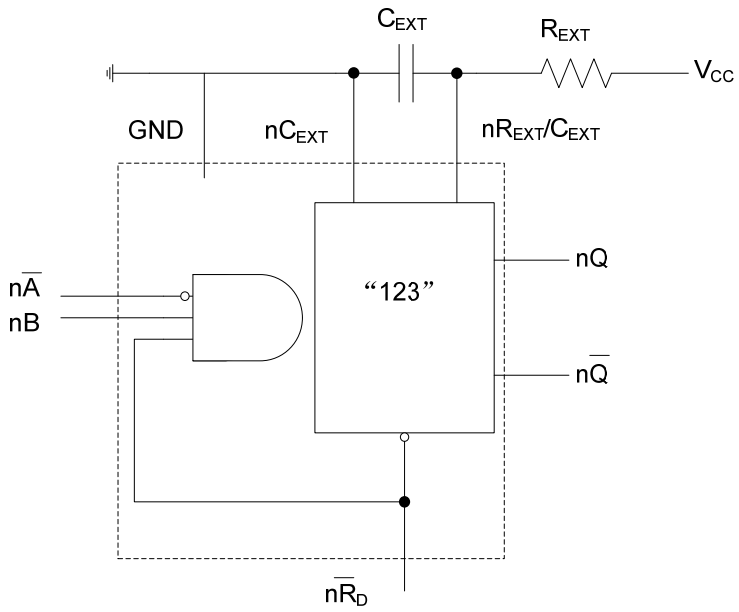
TEST CIRCUIT



■ APPLICATION INFORMATION

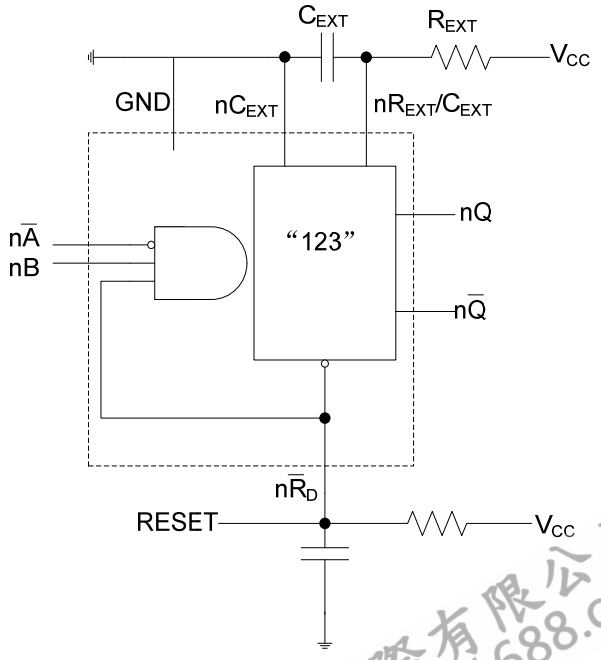
Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.



Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT}, this output can be eliminated using the circuit below.

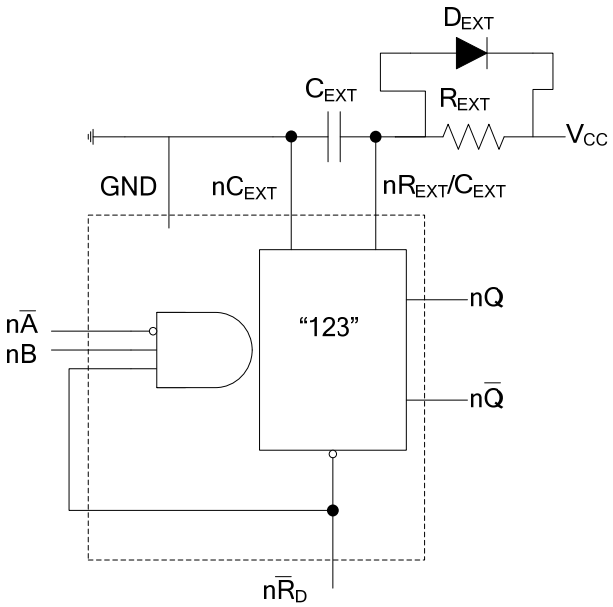


Power-up output pulse elimination circuit

■ APPLICATION INFORMATION(Cont.)

Power-down considerations

A large capacitor (C_{EXT}) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown below.



Power-down protection circuit