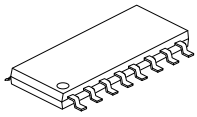
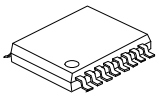
U74HC4046A

CMOS IC

PHASE LOCKED LOOP WITH VCO



SOP-16



TSSOP-16

■ DESCRIPTION

The **U74HC4046A** is a phase-locked-loop circuit including a linear voltage-controlled oscillator (VCO), three different phase comparators (PC1, PC2 and PC3), a common signal input amplifier and a common comparator input.

The signal can be directly coupled to large voltage signals or with a series capacitor coupled to small voltage signals. Small voltage signals can be kept within the linear region of the input amplifiers with a self-bias input circuit. The **U74HC4046A** and a passive low-pass filter form a second-order loop PLL. With a linear op-amp, the VCO achieves excellent linearity.

The VCO requires an external capacitor and resistor. R1 (between R1 and GND) and capacitor C1 (between C1A and C1B) determine the frequency range of the VCO. R2 (between R2 and GND) enables the VCO to have a frequency offset if required.

For the high input impedance of the VCO, the design of low-pass filters is simplified, and the designer has a wide choice of resistor/capacitor ranges. At pin 10 (DEM_{OUT}), a demodulator output of the VCO input voltage is provided in order not to load the low-pass filter. In conventional techniques, the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, but the DEM_{OUT} voltage of U74HC4046 equals the VCO input voltage. When DEM_{OUT} is used, a load resistor (RS) should be connected from DEM_{OUT} to GND; but if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly or via a frequency-divider to the comparator input ($COMP_{IN}$). If the VCO input is held at a constant DC level, the VCO output signal has a duty factor of 50% (maximum expected deviation 1%). A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

■ FEATURES

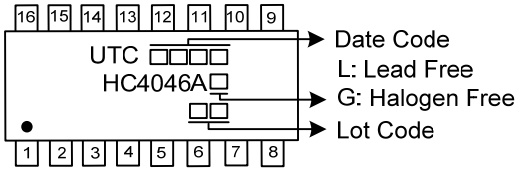
* Low Power Consumption
* Operating Power Supply Voltage Range: Digital Section 2.0 to 6.0 V
  VCO Section 3.0 to 6.0 V
* Up to 17 MHz (typ.) Centre Frequency at V_{CC} = 4.5 V
* Excellent VCO Frequency Linearity
* VCO-Inhibit Control For ON/OFF Keying and for Low Standby Power Consumption
* Minimal Frequency Drift
* Three Phase Comparators: EXCLUSIVE-OR;
  Edge-Triggered JK Flip-Flop;
  Edge-Triggered RS Flip-Flop
* Zero Voltage Offset due to OP-Amp Buffering
* Standard Output Capability
* MSI I_{CC} Category

■ ORDERING INFORMATION

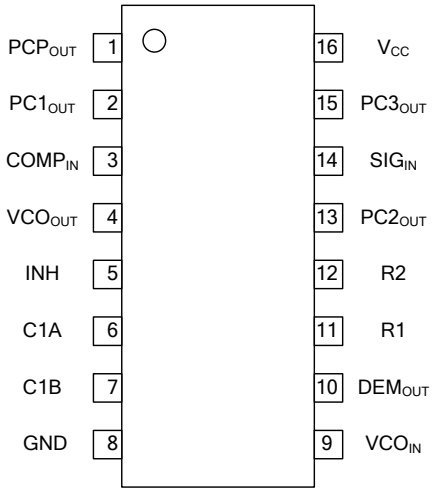
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC4046AL-S16-R	U74HC4046AG-S16-R	SOP-16	Tape Reel
U74HC4046AL-P16-R	U74HC4046AG-P16-R	TSSOP-16	Tape Reel

U74HC4046AG-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16, P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

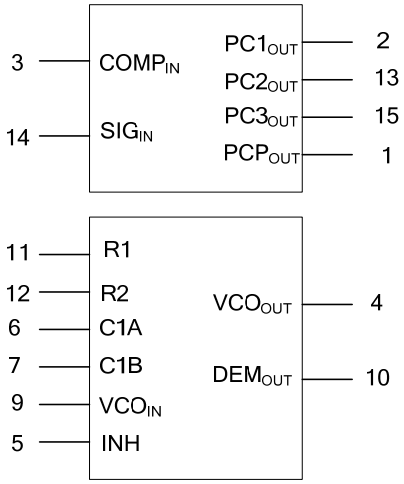
■ MARKING



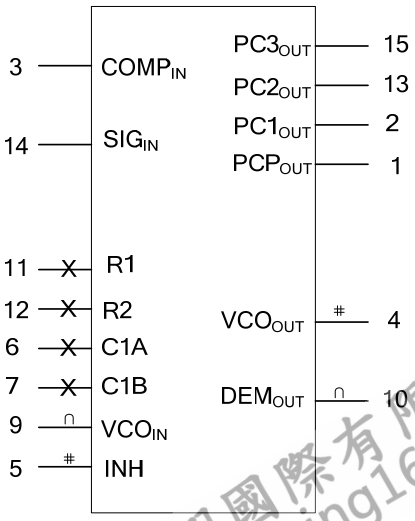
■ PIN CONFIGURATION



■ LOGIC SYMBOL



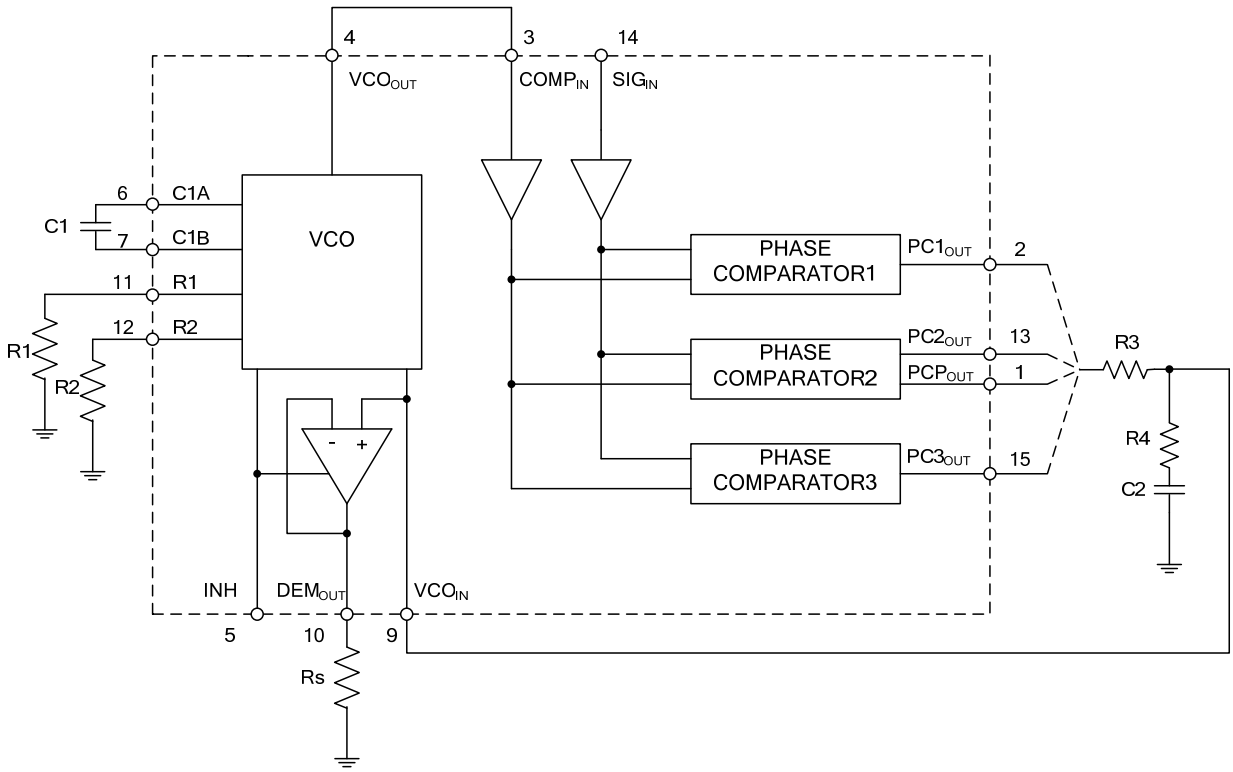
■ IEC SYMBOL



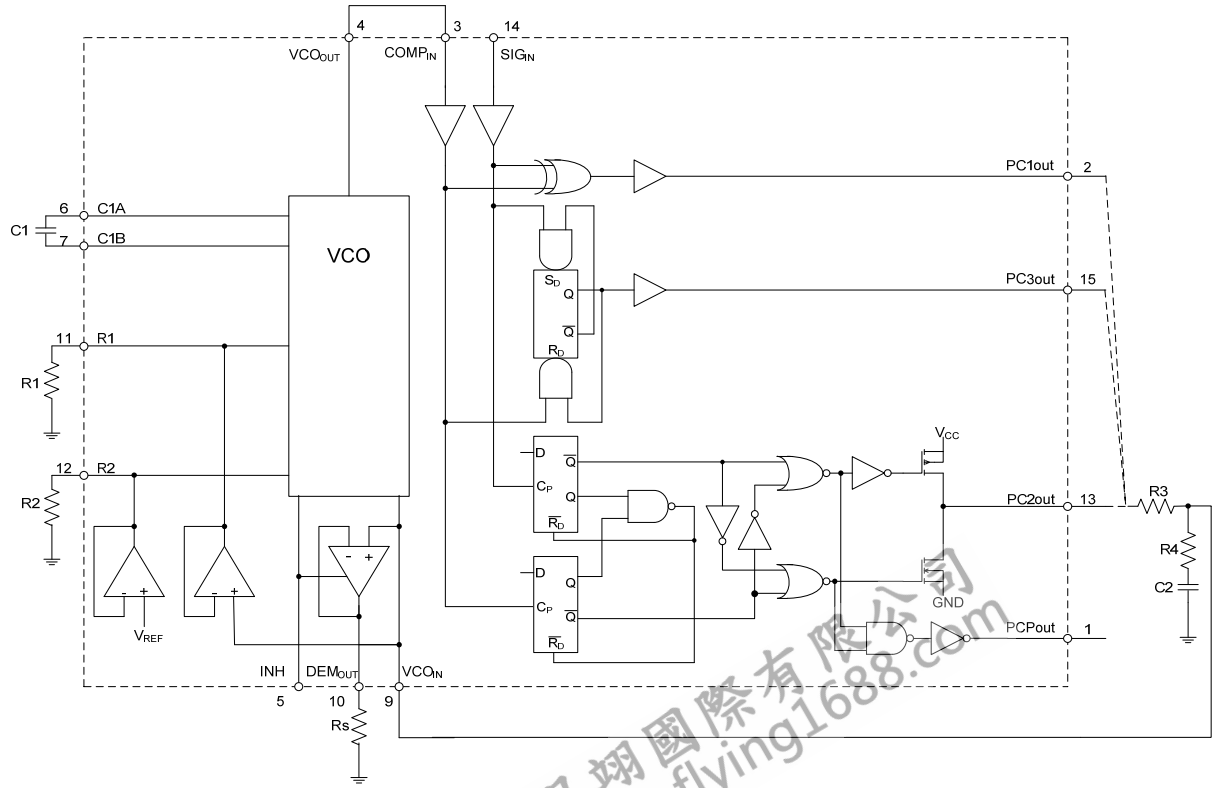
■ PIN DESCRIPTION

PIN NO	SYMBOL	FUNCTION
1	PCP_{OUT}	Phase comparator pulse output
2	$PC1_{OUT}$	Phase comparator 1output
3	$COMP_{IN}$	Comparator input
4	VCO_{OUT}	VCO output
5	INH	Inhibit input
6	$C1_A$	Capacitor C1 connection A
7	$C1_B$	Capacitor C1 connection B
8	GND	Ground
9	VCO_{IN}	VCO input
10	DEM_{OUT}	Demodulator output
11	R1	Resistor R1 connection
12	R2	Resistor R2 connection
13	$PC2_{OUT}$	Phase comparator 2 output
14	SIG_{IN}	Signal input
15	$PC3_{OUT}$	Phase comparator 3 output
16	V_{CC}	Positive supply voltage

■ FUNCTIONAL DIAGRAM



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	V_{CC}		-0.5		+7	V
DC Input Diode Current	$\pm I_{IK}$	for V_{IN} <−0.5 V or V_{IN} > V_{CC} + 0.5 V			20	mA
DC Output Diode Current	$\pm I_{OK}$	for V_{OUT} <−0.5 V or V_{OUT} > V_{CC} + 0.5 V			20	mA
DC Output Source or Sink Current	$\pm I_O$	for −0.5 V < V_{OUT} < V_{CC} + 0.5 V			25	mA
DC V_{CC} or GND Current	$\pm I_{CC}$, $\pm I_{GND}$				50	mA
Power Dissipation per Package Plastic DIL	P_D	for temperature range: − 40 to +125 °C above +70 °C: derate linearly with 12 mW/K			750	mW
Power Dissipation per Package Plastic Mini-Pack(SO)		for temperature range: − 40 to +125 °C above +70 °C: derate linearly with 8 mW/K			500	mW
Storage Temperature Range	T_{STG}		-65		+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	V_{CC}		3.0	5.0	6.0	V
DC Supply Voltage if VCO Section is not used	V_{CC}		2.0	5.0	6.0	V
DC Input Voltage Range	V_{IN}		0		V_{CC}	V
DC Output Voltage Range	V_{OUT}		0		V_{CC}	V
Input Rise and Fall Times (pin 5)	t_R, t_F	V_{CC} = 2.0 V		6.0	1000	ns
		V_{CC} = 4.5 V		6.0	500	ns
		V_{CC} = 6.0 V		6.0	400	ns
Ambient Operating Temperature	T_{OPR}		-40		+125	°C

■ QUICK REFERENCE DATA (GND = 5V; T = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCO Centre Frequency	f_o	C1=40pF; R1=3kΩ; V_{CC}=5V		19		MHz
Input Capacitance (Pin 5)	C_{IN}			3.5		pF
Power Dissipation Capacitance per Package	C_{PD}	(Note)		24		pF

Note : C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \sum (C_L \times V_{CC}{}^2 \times f_O)$$

where: f_i = input frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
f_o =output frequency in MHz;
$\sum (C_L \times V_{CC}{}^2 \times f_O)$ = sum of outputs.

■ DC CHARACTERISTICS (T_A =25°C , unless otherwise specified)

Quiescent Supply Current (Voltages are referenced to GND (ground = 0 V))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Quiescent Supply Current (VCO Disabled)	I_{CC}	V_{CC}=6.0V	Pins 3, 5 and 14 at V_{CC}; Pin 9 at GND; I_{IN} at pins 3 and 14 to be excluded			8.0	μA

Phase Comparator Section

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC Coupled (HIGH Level Input Voltage SIG_{IN}, $COMP_{IN}$)	V_{IH}	V_{CC}=2.0V		1.5	1.2		V
		V_{CC}=4.5V		3.15	2.4		
		V_{CC}=6.0V		4.2	3.2		
DC Coupled (LOW Level Input Voltage SIG_{IN}, $COMP_{IN}$)	V_{IL}	V_{CC}=2.0V			0.8	0.5	V
		V_{CC}=4.5V			2.1	1.35	
		V_{CC}=6.0V			2.8	1.8	
HIGH Level Output Voltage (PCP_{OUT}, PC_{nOUT})	V_{OH}	V_I=V_{IH} or V_{IL}, - I_{OUT} = 20μA	V_{CC}=2.0V	1.9	2.0		V
			V_{CC}=4.5V	4.4	4.5		
			V_{CC}=6.0V	5.9	6.0		
HIGH Level Output Voltage (PCP_{OUT}, PC_{nOUT})	V_{OH}	V_I=V_{IH} or V_{IL},	V_{CC}=4.5V, - I_O = 4.0 mA	3.98	4.32		V
			V_{CC}=6.0V ,- I_O = 5.2 mA	5.48	5.81		
LOW Level Output Voltage (PCP_{OUT}, PC_{nOUT})	V_{OL}	V_I=V_{IH} or V_{IL}, - I_{OUT} = 20μA	V_{CC}=2.0V		0	0.1	V
			V_{CC}=4.5V		0	0.1	
			V_{CC}=6.0V		0	0.1	
LOW Level Output Voltage (PCP_{OUT}, PC_{nOUT})	V_{OL}	V_I=V_{IH} or V_{IL},	V_{CC}=4.5V , I_O = 4.0 mA		0.15	0.26	V
			V_{CC}=6.0V , I_O = 5.2 mA		0.16	0.26	
Input Leakage Current (SIG_{IN}, $COMP_{IN}$)	$\pm I_{IN}$	V_I = V_{CC} or GND	V_{CC}=2.0V			3.0	μA
			V_{CC}=3.0V			7.0	
			V_{CC}=4.5V			18.0	
			V_{CC}=6.0V			30.0	
3-State (OFF-state current $PC2_{OUT}$)	$\pm I_{OZ}$	V_{OUT} = V_{CC} or GND, V_I=V_{IH} or V_{IL}, V_{CC}=6.0V				0.5	μA
Input Resistance (SIG_{IN}, $COMP_{IN}$)	R_{IN}	V_{CC}=3.0V	V_{IN} at self-bias operating point; ΔV_I = 0.5V; (Fig. 7)		800		kΩ
		V_{CC}=4.5V			250		kΩ
		V_{CC}=6.0V			150		kΩ

VCO Section (Voltages are Referenced to GND (Ground = 0 V))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
HIGH Level Input Voltage INH	V_{IH}	V_{CC}=3.0V		2.1	1.7		V
		V_{CC}=4.5V		3.15	2.4		
		V_{CC}=6.0V		4.2	3.2		
LOW Level Input Voltage INH	V_{IL}	V_{CC}=3.0V			1.3	0.9	V
		V_{CC}=4.5V			2.1	1.35	
		V_{CC}=6.0V			2.8	1.8	
HIGH Level Output Voltage VCO_{OUT}	V_{OH}	V_I=V_{IH} or V_{IL}, - I_{OUT} = 20μA	V_{CC}=3.0V	2.9	3.0		V
			V_{CC}=4.5V	4.4	4.5		
			V_{CC}=6.0V	5.9	6.0		
HIGH Level Output Voltage VCO_{OUT}	V_{OH}	V_I=V_{IH} or V_{IL}	V_{CC}=4.5V, -I_{OUT} = 4.0 mA	3.98	4.32		V
			V_{CC}=6.0V, -I_{OUT} = 5.2 mA	5.48	5.81		
LOW Level Output Voltage VCO_{OUT}	V_{OL}	V_I=V_{IH} or V_{IL}, I_{OUT} = 20μA	V_{CC}=3.0V		0	0.1	V
			V_{CC}=4.5V		0	0.1	
			V_{CC}=6.0V		0	0.1	
LOW Level Output Voltage VCO_{OUT}	V_{OL}	V_I=V_{IH} or V_{IL}	V_{CC}=4.5V, I_{OUT} = 4.0 mA		0.15	0.26	V
			V_{CC}=6.0V, I_{OUT} = 5.2 mA		0.16	0.26	
LOW Level Output Voltage $C1_A$, $C1_B$	V_{OL}	V_I=V_{IH} or V_{IL}	V_{CC}=4.5V, I_{OUT} = 4.0 mA			0.4	V
			V_{CC}=6.0V, I_{OUT}=5.2 mA			0.4	V
Input Leakage Current(INH, VCO_{IN})	$\pm I_{IN}$	V_{CC}=6.0V, V_I=V_{CC} or GND				0.1	μA

■ DC CHARACTERISTICS(Cont.)

VCO Section (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resistance Range	R1	V_{CC}=3.0V		3.0		300	kΩ
		V_{CC}=4.5V		3.0		300	
		V_{CC}=6.0V		3.0		300	
	R2	V_{CC}=3.0V	(Note)	3.0		300	kΩ
		V_{CC}=4.5V		3.0		300	
		V_{CC}=6.0V		3.0		300	
Capacitor Range	C1	V_{CC}=3.0V		40			pF
		V_{CC}=4.5V		40			
		V_{CC}=6.0V		40			
Operating Voltage Range at VCO_{IN}	V_{VCOIN}	V_{CC}=3.0V	Over the range specified for R1; for linearity (Fig10)	1.1		1.9	V
		V_{CC}=4.5V		1.1		3.4	
		V_{CC}=6.0V		1.1		4.9	

Note: The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is > 10 kΩ.

Demodulator Section (Voltages are Referenced to GND (Ground = 0 V))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resistor Range	R_S	V_{CC}=3.0V	At R_S > 300 kΩ the leakage current can influence V_{DEMOUT}	50		300	kΩ
		V_{CC}=4.5V		50		300	
		V_{CC}=6.0V		50		300	
Offset Voltage VCO_{IN} to V_{DEMOUT}	V_{OFF}	V_{CC}=3.0V	V_I = V_{VCOIN} =1/2 V_{CC}; values taken over R_S range		±30		mV
		V_{CC}=4.5V			±20		
		V_{CC}=6.0V			±10		
Dynamic Output Resistance at DEM_{OUT}	R_D	V_{CC}=3.0V	V_{DEMOUT} = 1/2 V_{CC}		25		Ω
		V_{CC}=4.5V			25		
		V_{CC}=6.0V			25		

■ AC CHARACTERISTICS (T_A =25°C , unless otherwise specified)

Phase Comparator Section (GND = 0 V; $t_R = t_F$ =6ns; C_L = 50pF)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$	t_{PHL}/ t_{PLH}	V_{CC}=2.0V	Fig.8		63	200	ns
		V_{CC}=4.5V			23	40	
		V_{CC}=6.0V			18	34	
Propagation Delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}	t_{PHL}/ t_{PLH}	V_{CC}=2.0V	Fig.8		96	340	ns
		V_{CC}=4.5V			35	68	
		V_{CC}=6.0V			28	58	
Propagation Delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$	t_{PHL}/ t_{PLH}	V_{CC}=2.0V	Fig.8		77	270	ns
		V_{CC}=4.5V			28	54	
		V_{CC}=6.0V			22	46	
3-State Output Enable Time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PZH}/ t_{PZL}	V_{CC}=2.0V	Fig.9		83	280	ns
		V_{CC}=4.5V			30	56	
		V_{CC}=6.0V			24	48	
3-State Output Disable Time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PHZ}/ t_{PLZ}	V_{CC}=2.0V	Fig.9		99	325	ns
		V_{CC}=4.5V			36	65	
		V_{CC}=6.0V			29	55	
Output Transition Time	t_{PHZ}/ t_{PLZ}	V_{CC}=2.0V	Fig.8		19	75	ns
		V_{CC}=4.5V			7	15	
		V_{CC}=6.0V			6	13	
AC Coupled Input Sensitivity (Peak-To-Peak Value) at SIG_{IN} or $COMP_{IN}$	$V_{IN(P-P)}$	V_{CC}=2.0V	f_i = 1MHz		9		mV
		V_{CC}=3.0V			11		
		V_{CC}=4.5V			15		
		V_{CC}=6.0V			33		

VCO Section (GND = 0 V; $t_R = t_F$ = 6 ns; C_L = 50 pF)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency Stability with Temperature Change	Δf/T	V_{CC}=3.0V	V_{IN} = V_{VCOIN} = 1/2 V_{CC}; R1 = 100 kΩ; R2 = ∞; C1= 100 pF		0.2		%/K
		V_{CC}=4.5V			0.15		
		V_{CC}=6.0V			0.14		
VCO Centre Frequency (duty Factor = 50%)	f_o	V_{CC}=3.0V	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ;R2 = ∞; C1 = 40 pF	7.0	10.0		MHz
		V_{CC}=4.5V		11.0	17.0		
		V_{CC}=6.0V		13.0	21.0		
VCO Frequency Linearity	Δf_{VCO}	V_{CC}=3.0V	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF;(Fig.10)		1.0		%
		V_{CC}=4.5V			0.4		
		V_{CC}=6.0V			0.3		
Duty Factor at VCO_{OUT}	δ_{VCO}	V_{CC}=3.0V			50		%
		V_{CC}=4.5V			50		
		V_{CC}=6.0V			50		

■ PHASE COMPARATORS

If the signal swing is between the standard HC family input logic levels, the signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. To obtain the maximum locking range, the signal and comparator input frequencies (f_I) must have a 50% duty factor.

The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

Where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The phase comparator gain is: $K_P = \frac{V_{CC}}{\pi}$ (V / r)

As shown in Fig.1, the average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}) is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$). The average of V_{DEMOUT} is equal to $V_{CC}/2$ when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_O). As shown in Fig.2 it is the typical waveforms for the PC1 loop locked at f_O.

$$V_{DEMOUT} = V_{PC1OUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$$

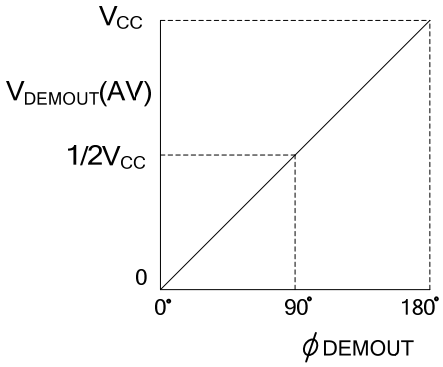


Fig.1 Phase comparator 1: average output voltage versus input phase difference.

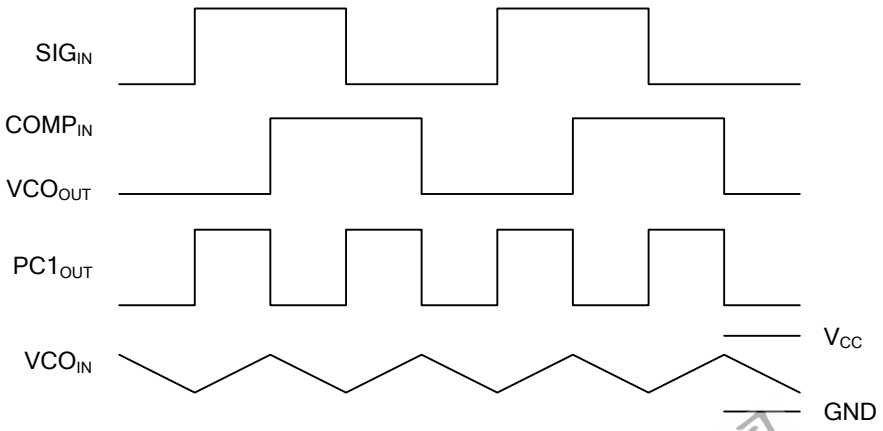


Fig.2 Typical waveforms for PLL using phase comparator 1, loop locked at f_O.

The frequency capture range ($2f_c$) is he frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the low-pass filter characteristics determine the capture range which can be made as large as the lock range.

This configuration retains lock even with very noisy input signals. Typical behavior of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

■ PHASE COMPARATORS (Cont.)

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. If the PLL is using the comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 is comprised of two D-type flip-flops, control-gating and a 3-state output stage. The circuit function is as an up-down counter (Logic Diagram) for SIG_{IN} causes an up-count and $COMP_{IN}$ causes a down-count.

The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is: $K_P = \frac{V_{CC}}{4\pi}(V/r)$

As shown in Fig.3, V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$. Typical waveforms for the PC2 loop locked at f_o are shown in Fig.4.

$$V_{DEMOUT} = V_{PC2OUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$$

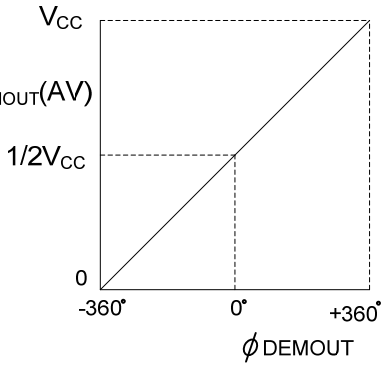


Fig.3 Phase comparator 2: average output voltage versus input phase difference.

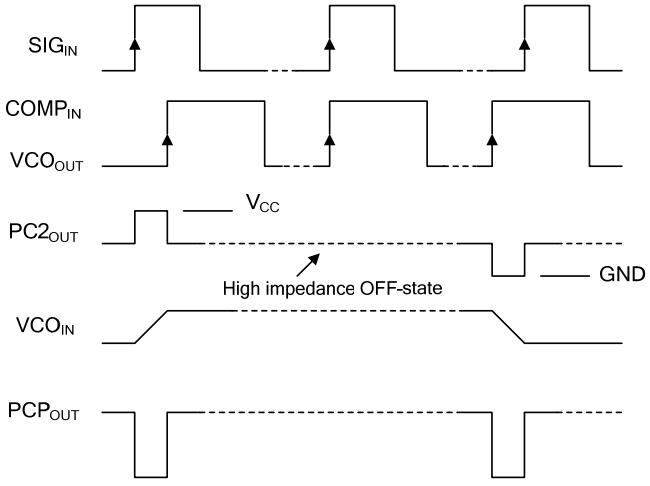


Fig.4 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

If the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). If the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

If the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are "OFF" (3-state). If the frequency of SIG_{IN} is lower than that of $COMP_{IN}$, the n-type driver that is held "ON" for most of the cycle. Then the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable state the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in the condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level, and it indicates a locked condition.

For PC2, there is no phase difference between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. And as the low-pass filter, the power dissipation is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and this is independent of the low-pass filter. The VCO adjusts to its lowest frequency via PC2 when no signal present at SIG_{IN}.

■ PHASE COMPARATORS (Cont.)

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. If this comparator is used, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_j$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where $V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The phase comparator gain is: $K_P = \frac{V_{CC}}{2\pi}$ (V / r)

As shown in Fig.5, the average output voltage from PC3, fed to the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$. As shown in Fig.6, it is the typical waveforms for the PC3 loop locked at f_o.

$$V_{DEMOUT} = V_{PC3OUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$$

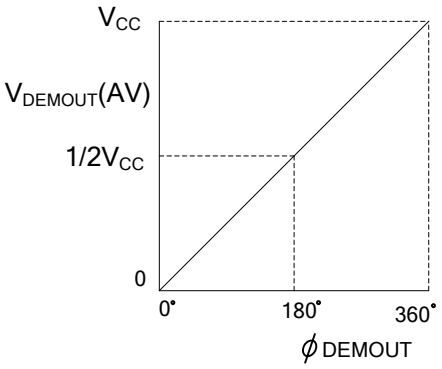


Fig.5 Phase comparator 3: average output voltage versus input phase difference.

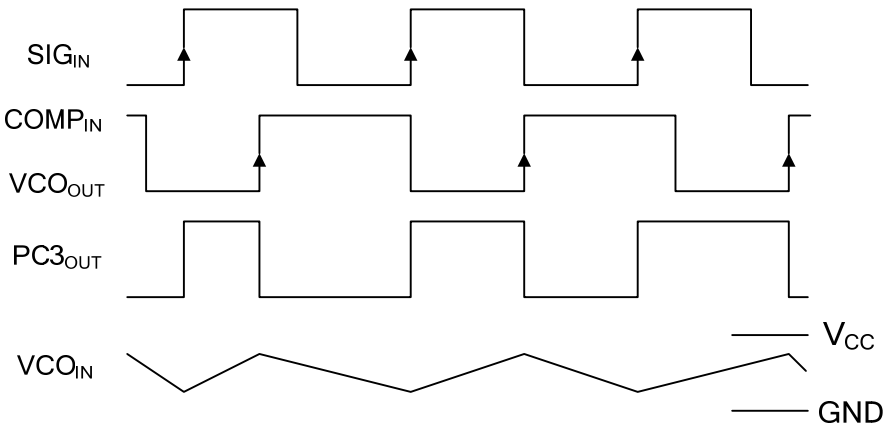


Fig.6 Typical waveforms for PLL using phase comparator 3, loop locked at f_o.

The phase-to-output response characteristic of PC3 (Fig.5) differs from that of PC2, as the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0^o and 360^o and 180^o is the centre frequency. And the voltage swing of PC3 is greater than that of PC2 for input phase differences, but as a consequence the ripple content of VCO input signal is higher. Both of the PLL lock range and capture range of this type of phase comparator are dependent on the low-pass filter. The VCO adjusts to its lowest frequency via PC3, when no signal present at SIG_{IN}.

■ FIGURE REFERENCES FOR DC CHARACTERISTICS

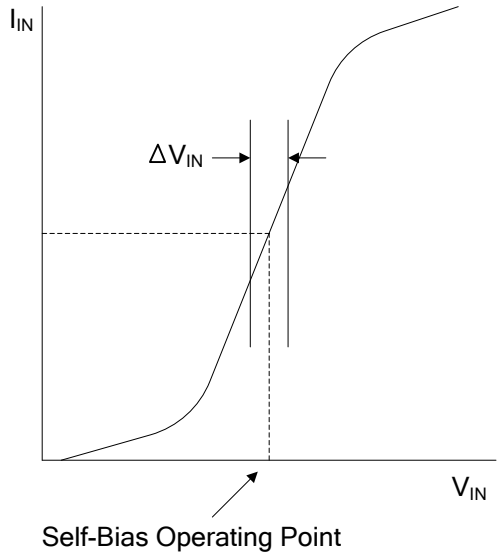


Fig.7 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

■ AC WAVEFORMS

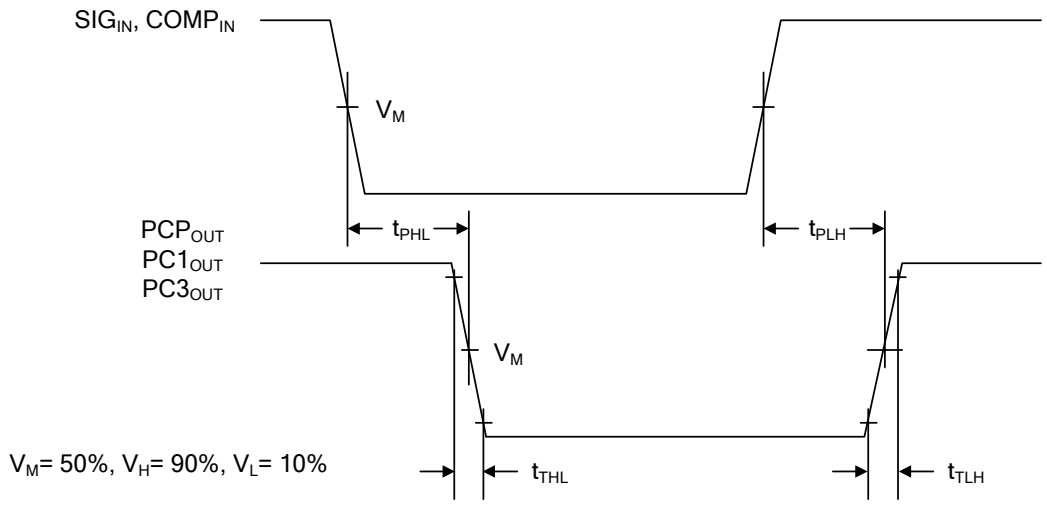
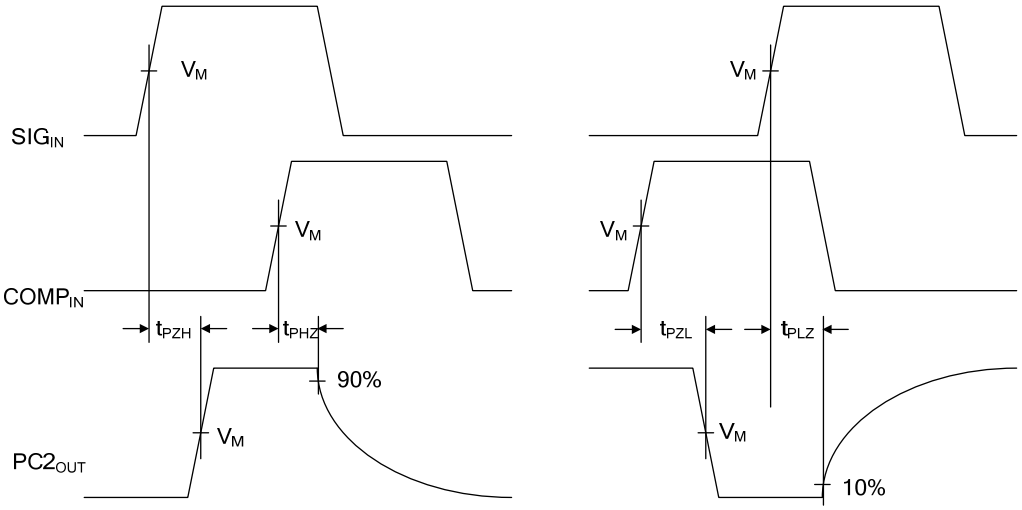


Fig.8 Waveforms showing input (SIG$_{IN}$, COMP$_{IN}$) to output (PCP$_{OUT}$, PC1$_{OUT}$, PC3$_{OUT}$) propagation delays and the output transition times.



V_M= 50%, V_H= 90%, V_L= 10%

Fig.9 Waveforms showing the 3-state enable and disable times for PC2$_{OUT}$.

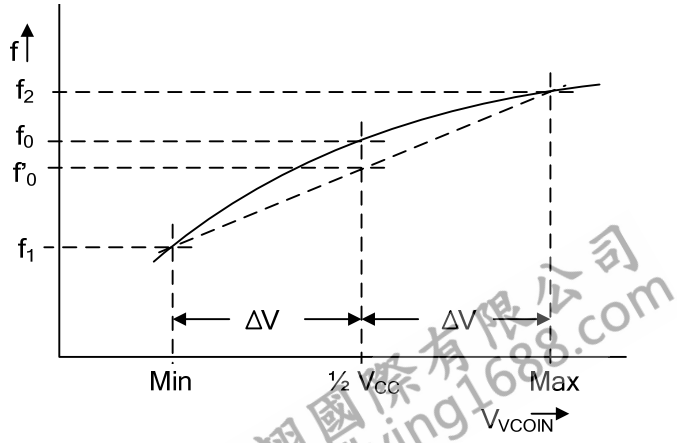


Fig.10 Definition of VCO frequency linearity: ΔV = 0.5 V over the V_{CC} range:
For VCO linearity $f'_0 = (f_1+f_2)/2$, linearity $(f'_0-f_0)/f'_0 \times 100\%$

■ APPLICATION INFORMATION

This is a reference for the values of external components to be used with the **U74HC4046A** in a PLL system. The ranges of the values of the components:

Component	Value
R1	3 kΩ ~ 300 kΩ
R2	3 kΩ ~ 300 kΩ
R1+R2	Parallel value > 2.7 kΩ
C1	Greater than 40 pF

VCO Frequency Without Extra Offset (Phase comparator: PC1, PC2 or PC3)

Frequency Characteristic:

With R2 = ∞ and R1 between 3 kΩ and 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.11 (Due to R1, C1 time constant a small offset remains when R2 = ∞).

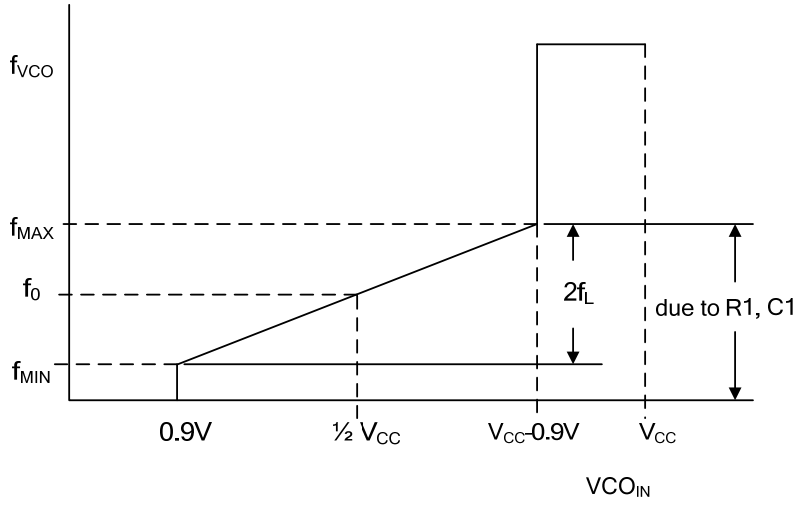


Fig.11 Frequency characteristic of VCO operating without offset:
f_0 = centre frequency; $2f_L$ = frequency lock range.

■ APPLICATION INFORMATION (Cont.)

VCO Frequency with Extra Offset (Phase Comparator: PC1, PC2 or PC3)
Frequency characteristic:
With R1 and R2 between 3 kΩ and 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.12.

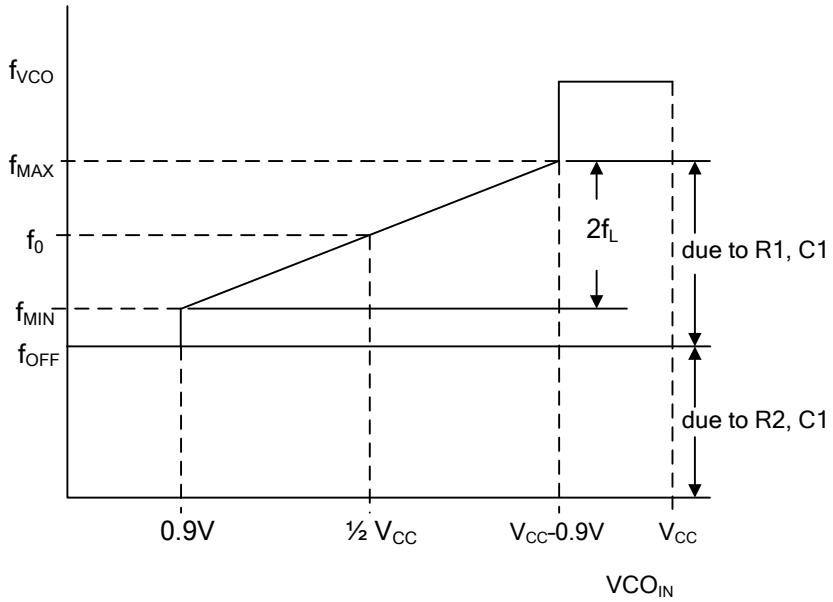


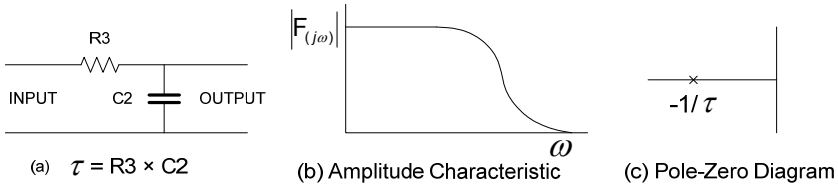
Fig.12 Frequency characteristic of VCO operating with offset:
f_0 = centre frequency; $2f_L$ = frequency lock range.
PC1, PC2 or PC3
Selection of R1, R2 and C1
Given f_o and f_L, determine the value of R1×C1
Calculate f_{OFF} from the equation $f_{OFF} = f_O - 1.6f_L$
Obtain the values of C1 and R2
Calculate the value of R1 from the value of C1 and R1×C1.

Subject	Phase comparator	Design considerations
PLL Conditions with no Signal at the SIG_{IN} Input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCONIN} = 1/2 V_{CC} (Fig.1).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = -360° and V_{VCONIN} = min. (Fig.3).
	PC3	VCO adjusts to f_o with ϕ_{DEMOUT} = -360° and V_{VCONIN} = min. (Fig.5).

■ APPLICATION INFORMATION(Cont.)

PLL Frequency Capture Range (Phase comparator: PC1, PC2 or PC3)

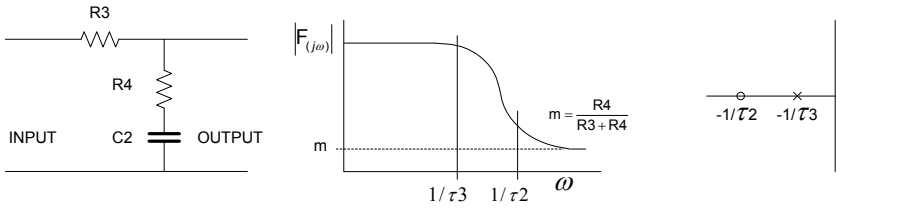
Loop filter component selection



(a) τ = R3 × C2 (b) Amplitude Characteristic (c) Pole-Zero Diagram

A small capture range ($2f_C$) is obtained if $2f_C \approx \frac{1}{\pi}\sqrt{2\pi f_L / \tau}$

Fig.13 Simple loop filter for PLL without offset; R3 ⩾ 500 Ω.



(a) τ1 = R3 × C2
τ2 = R4 × C2
τ3 = (R3 + 4)× C2

(b) Amplitude Characteristic (c) Pole-Zero Diagram

Fig.14 Simple loop filter for PLL with offset; R3 + R4 ⩾ 500 Ω.

Subject	Phase comparator	Design considerations
PLL Locks on Harmonics at Centre Frequency	PC1 or PC3	Yes
	PC2	No
Noise Rejection at Signal Input	PC1	High
	PC2 or PC3	Low
AC Ripple Content when PLL is Locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°
	PC3	$f_r = f_i$, large ripple content at ϕ_{DEMOUT} = 180°

■ PLL DESIGN EXAMPLE

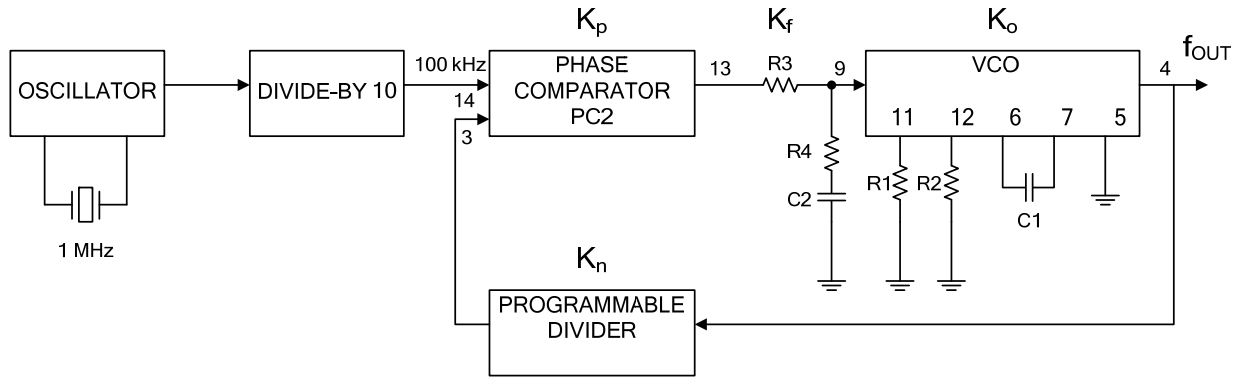


Fig.15 Frequency Synthesizer.

The parameters of the frequency synthesizer in Fig.15:
Output frequency: 2 MHz to 3 MHz
Frequency steps: 100kHz
Settling time: 1ms
Overshoot: < 20%

The **Open-Loop Gain** is: $H(s)\times G(s) = K_p \times K_f \times K_o \times K_n$

Where: K_p = phase comparator gain
K_f = low-pass filter transfer gain
K_o = K_v/s VCO gain
K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{Min} = \frac{f_{out}}{f_{step}} = \frac{2MHz}{100kHz} = 20$$

$$N_{Max} = \frac{f_{out}}{f_{step}} = \frac{3MHz}{100kHz} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable). The values can be determined using the information in the section “DESIGN CONSIDERATIONS”.
With f_o = 2.5MHz and f_L =500 kHz this gives the following values (V_{CC} = 5.0 V):
R1 = 10 kΩ; R2 = 10 kΩ; C1 = 500 pF

The VCO gain is: $$K_V = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} = \frac{1MHz}{3.2} \times 2\pi \approx 2 \times 10^6 r/s/V$$

The gain of the phase comparator is: $$K_p = \frac{V_{CC}}{4\pi} = 0.4V/r$$

The transfer gain of the filter is given by: $$K_f = \frac{1+\tau_2 S}{1+(\tau_1+\tau_2)S}$$

Where: $\tau_1 = R3C2$ and $\tau_2 = R4C2$

The characteristics equation is: 1 + H(S) × G(S) = 0

This results in: $$S^2 + \frac{1+K_p \times K_v \times K_n \times \tau_2}{(\tau_1+\tau_2)} S + \frac{K_p \times K_v \times K_n}{(\tau_1+\tau_2)} = 0$$

The natural frequency ω_n is defined as follows: $$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1+\tau_2)}}$$

Damping Value ξ is Defined as follows: $$\zeta = \frac{1}{2\omega_n} \times \frac{1+K_p \times K_v \times K_n \times \tau_2}{(\tau_1+\tau_2)}$$