



U74HCT4094

CMOS IC

8-STAGE SHIFT&STORE BUS REGISTER

DESCRIPTION

The **U74HCT4094** consists of an 8-stage shift register and 8-stage D-type latch with 3-stage parallel outputs. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage QS1 can be used to cascade several devices.

The output of QS1 is transferred to a second output(QS2) on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch which latches data on the negative going transition of the Strobe input signal. When the strobe input is held high, data propagates through the latch to a 3-state output buffer.

The buffer is enabled when Output Enable input is taken high.

FEATURES

- * Operate from 4.5V to 5.5V
- * Low Input Current: 0.1µA
- * High Noise Immunity Characteristic of CMOS Devices
- * Inputs are TTL Voltage Compatible.

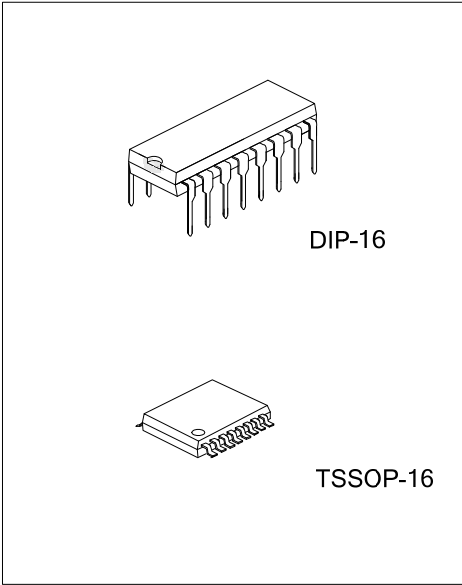
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT4094L-D16-T	U74HCT4094G-D16-T	DIP-16	Tube
U74HCT4094L-P16-R	U74HCT4094G-P16-R	TSSOP-16	Tape Reel

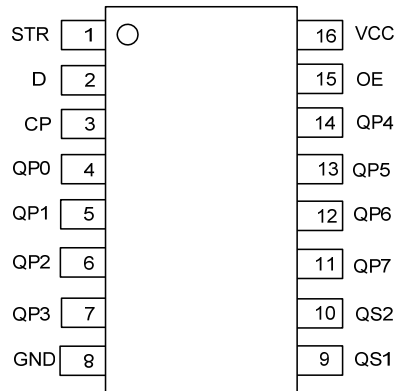
<p>U74HCT4094G-D16-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D16: DIP-16, P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

DIP-16	TSSOP-16
<p>Date Code UTC □□□□ L: Lead Free U74HCT4094 □ G: Halogen Free □□ Lot Code</p>	<p>Date Code UTC □□□□ L: Lead Free U74HCT4094 □ G: Halogen Free □□ Lot Code</p>



■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	QP7
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	QPn-1	Q'6	NC
↑	H	H	H	H	QPn-1	Q'6	NC
↓	H	H	H	NC	NC	NC	QP7

Note: H : HIGH voltage level; L : LOW voltage level.

X : Don't care. High impedance OFF-state.

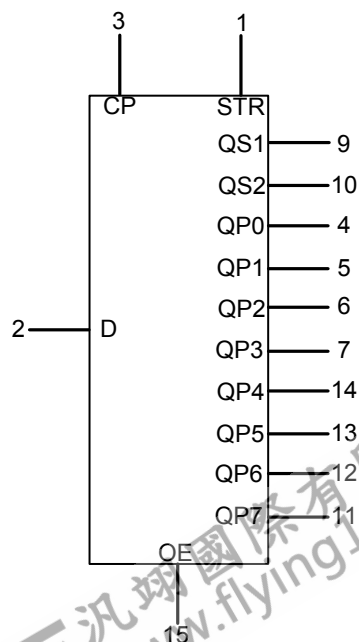
NC: No change.

↑ : Low-to-High CP transition.

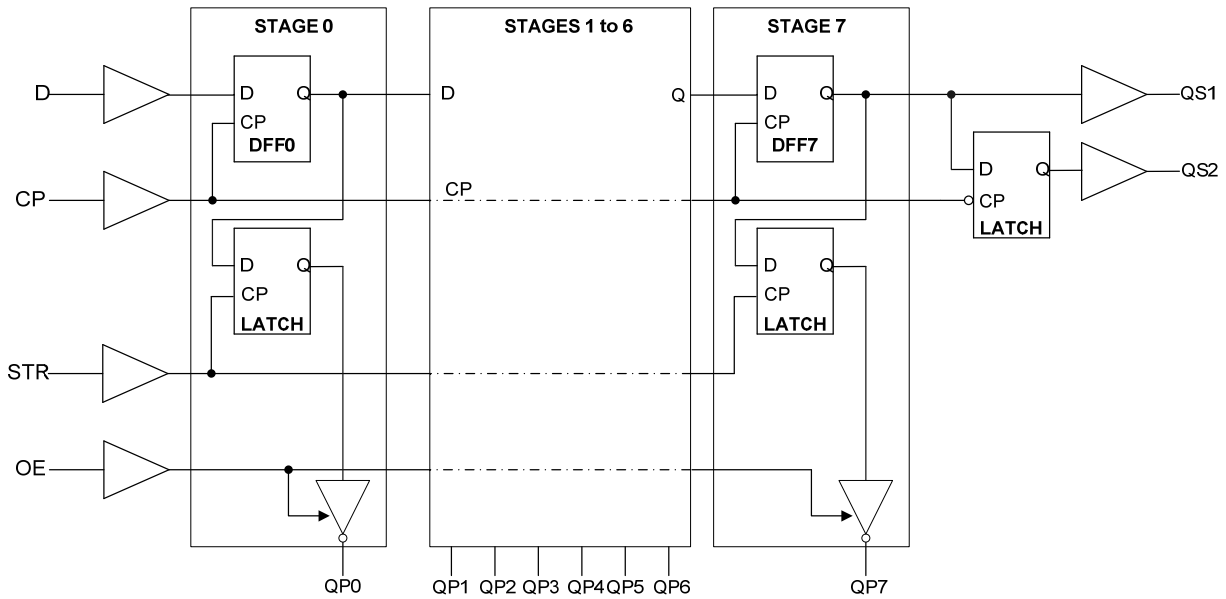
↓ : High-to-Low CP transition.

Q'6: the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

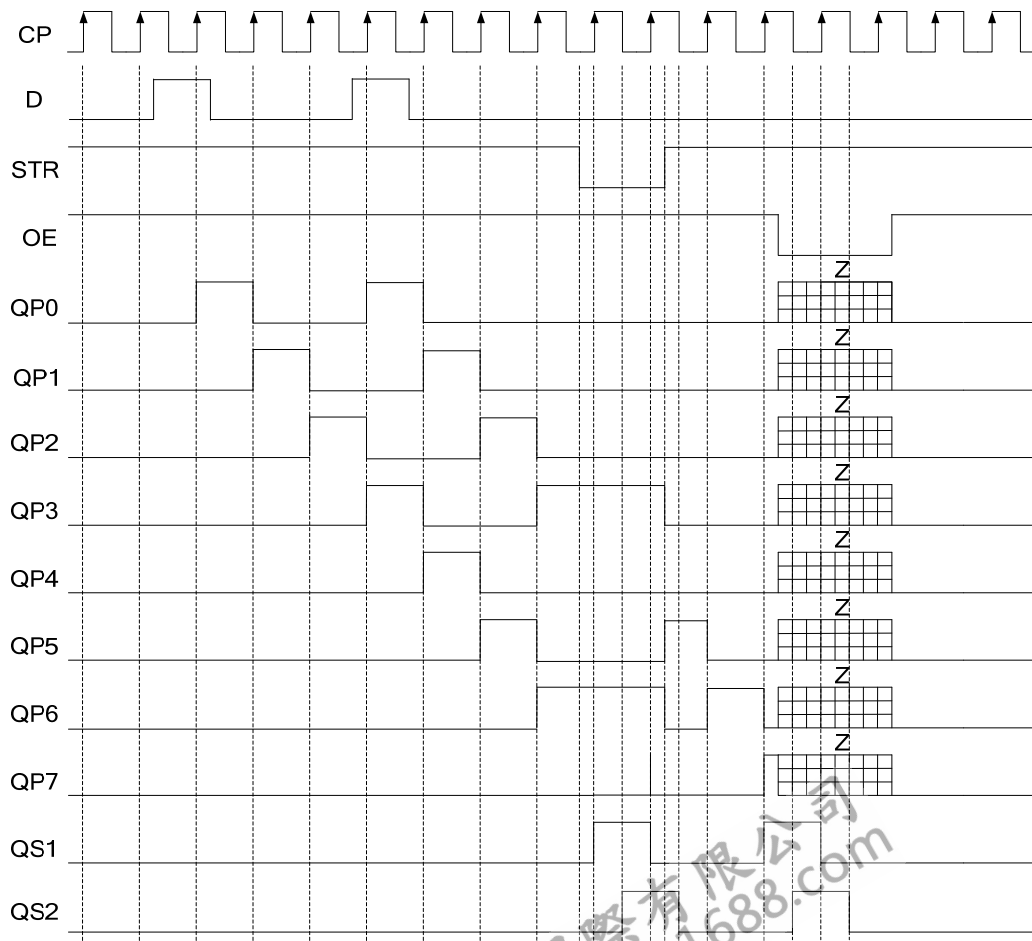
■ LOGIC SYMBOL



LOGIC DIAGRAM



TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 1.5$	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
V_{CC} or GND Current	I_{CC}	±50	mA
Input Current	I_{IN}	±20	mA
Output Current	I_{OUT}	±25	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	4.5		5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+125	°C
Input Rise or Fall Times	t_R, t_F	$V_{CC}=4.5V$ to 5.5V			500	ns

■ ELECTRICAL CHARACTERISTICS($T_A=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	V_{IH}	$V_{CC}=4.5V$ to 5.5V	2.0	1.6		V
Low-level output voltage	V_{IL}	$V_{CC}=4.5V$ to 5.5V		1.2	0.8	V
High-Level Output Voltage,	V_{OH}	$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4			V
		$V_{CC}=4.5V, I_{OH}=-4mA$	3.98			V
Low-Level Output Voltage,	V_{OL}	$V_{CC}=4.5V, I_{OL}=20\mu A$			0.1	V
		$V_{CC}=4.5V, I_{OL}=4mA$			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=3V$ or GND			±0.1	μA
Output OFF -state current	I_{OZ}	$V_{CC}=5.5V, V_{OUT}=V_{CC}$ or GND			±0.5	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=3V$ or GND, $I_{OUT}=0$			4	μA
Additional Quiescent Supply Current	ΔI_{CC}	$V_{IN}=V_{CC}-2.1V,$ other inputs at V_{CC} or GND	STR	100	360	μA
			OE	150	540	
			CP	150	540	
			D	40	144	

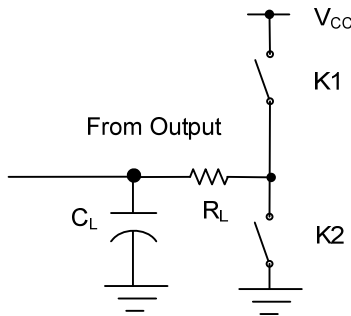
■ SWITCHING CHARACTERISTICS (T_A=25°C, see TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay from Input (CP) to Output(QS1)	t _{PHL} /t _{PLH}	V _{CC} =4.5V		23	39	ns
Propagation Delay from Input (CP) to Output(QS2)	t _{PHL} /t _{PLH}	V _{CC} =4.5V		21	36	ns
Propagation Delay from Input (CP) to Output (QPn)	t _{PHL} /t _{PLH}	V _{CC} =4.5V		25	43	ns
Propagation Delay from Input (STR) to Output (QPn)	t _{PHL} /t _{PLH}	V _{CC} =4.5V		22	39	ns
3-state Output Enable Time from Input (OE) to Output(QPn)	t _{PZH} /t _{PZL}	V _{CC} =4.5V		20	35	ns
3-State Output Disable Time from Input (OE) to Output(QPn)	t _{PHZ} /t _{PLZ}	V _{CC} =4.5V		21	35	ns
Output Transition Time(QSn、QPn)	t _{TLH} / t _{THL}	V _{CC} =4.5V		7	15	ns
Clock Pulse Width HIGH or LOW(CP)	t _W	V _{CC} =4.5V	16	7		ns
Strobe Pulse Width HIGH(STR)	t _W	V _{CC} =4.5V	16	5		ns
Set-up Time(D to CP)	t _{SU}	V _{CC} =4.5V	10	4		ns
Set-up Time(D to STR)	t _{SU}	V _{CC} =4.5V	20	9		ns
Hold Time(D to CP)	t _H	V _{CC} =4.5V	4	0		ns
Hold Time(D to STR)	t _H	V _{CC} =4.5V	0	-4		ns
Maximum Clock Pulse Frequency	f _(MAX)	V _{CC} =4.5V	30	80		MHz

■ OPERATING CHARACTERISTICS

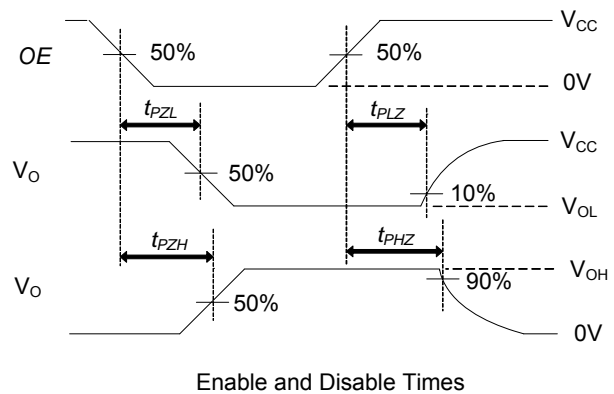
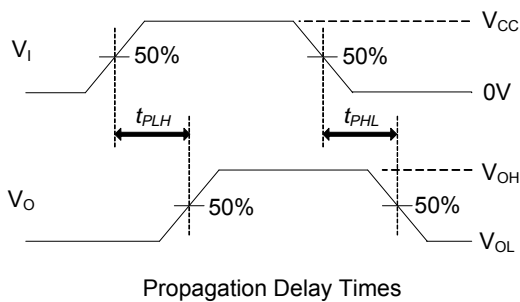
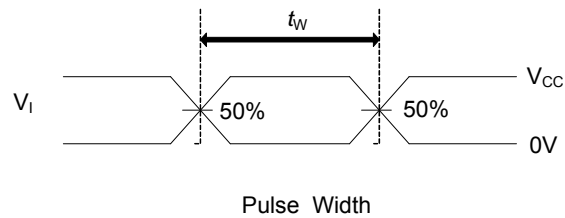
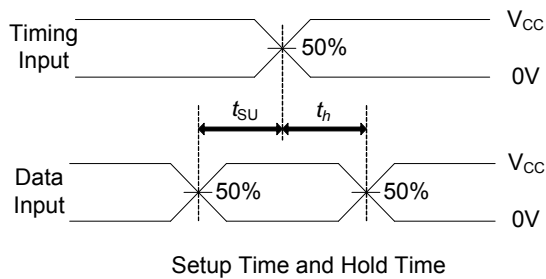
PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	C _{PD}	No Load	92	pF

TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

Note: $C_L = 50\text{pF}$, $R_L = 1\text{k}\Omega$



Note: C_L includes probe and jig capacitance.
 $P_{RR} \leq 10\text{MHz}$, $Z_o = 50\Omega$, $t_R \leq 6\text{ns}$, $t_F \leq 6\text{ns}$.

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