



U74HCT73

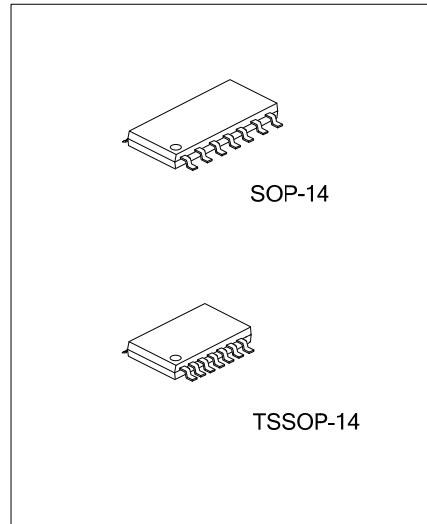
CMOS IC

DUAL J-K FLIP-FLOPS WITH CLEAR AND PRESET

DESCRIPTION

The **U74HCT73** is a dual J-K negative-edge-triggered flip-flop.

The clear (\overline{CLR}) input can reset the output at a low level, regardless of the level of others inputs. when the \overline{CLR} is inactive(high), data at the data inputs meeting the set-up time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Following the hold-time interval, data J and k inputs can be changed without affecting the levels at the outputs.



FEATURES

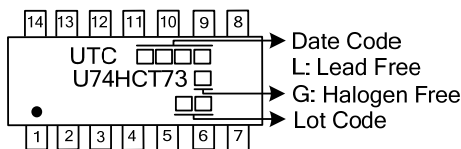
- * Wide supply voltage range from 4.5V to 5.5V
- * Low static power consumption; $I_{CC}=4\mu A$ (Max.)

ORDERING INFORMATION

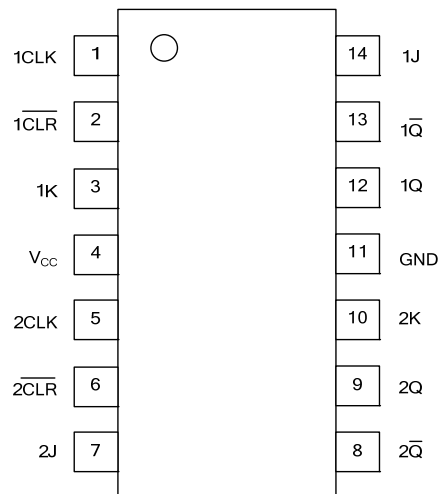
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT73L-S14-R	U74HCT73G-S14-R	SOP-14	Tape Reel
U74HCT73L-P14-R	U74HCT73G-P14-R	TSSOP-14	Tape Reel

<p>U74HCT73G-S14-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S14: SOP-14, P14: TSSOP-14</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

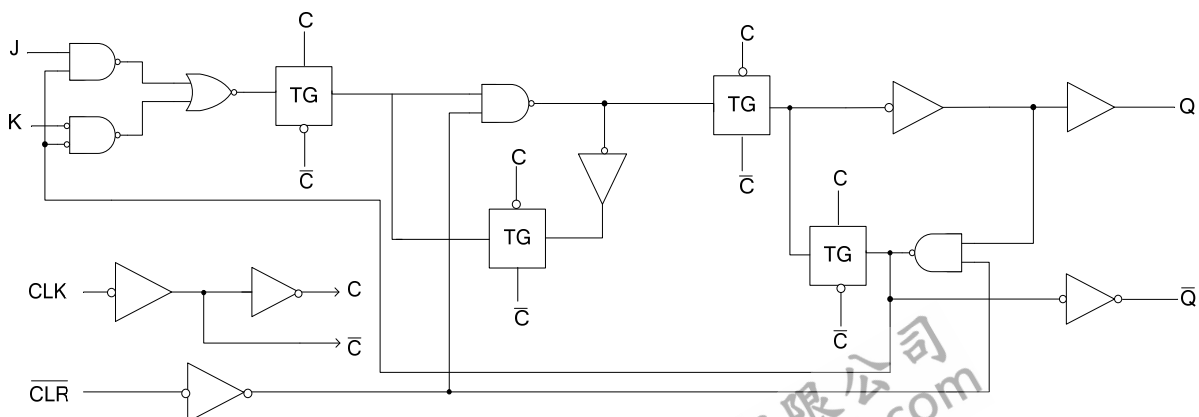


■ FUNCTION TABLE

INPUT				OUTPUT	
$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	X	X	X	L	H
H	↓	L	L	Q_0	\overline{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	\overline{Q}_0

Note: This configuration is unstable, as it is not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ return to high level.

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Note 2)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ $V_{CC}+0.5$	V
Output Voltage	V_{OUT}	Active Mode	-0.5 ~ $V_{CC}+0.5$	V
Continuous V_{CC} or GND Current	I_{CC}		±50	μA
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	±25	mA
Input Clamp Current	I_{IK}	$V_{IN}<0V$ or $V_{IN}>V_{CC}$	±20	mA
Output Clamp Current	I_{OK}	$V_{OUT}>V_{CC}$ or $V_{OUT}<0V$	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+85	°C
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$				500	ns

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-level Input Voltage	V_{IH}	$V_{CC}=4.5V \sim 5.5V$	2			V	
Low-level Input Voltage	V_{IL}	$V_{CC}=4.5V \sim 5.5V$			0.8	V	
High-Level Output Voltage	V_{OH}	$V_{CC}=4.5V$	$I_{OH}=-20\mu A$	4.4	4.999	V	
			$I_{OH}=-4mA$	3.98		V	
Low-Level Output Voltage	V_{OL}	$V_{CC}=4.5V$	$I_{OL}=20\mu A$		0.001	0.1	V
			$I_{OL}=4mA$			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND			±0.1	μA	
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0V$			4	μA	
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=4.5V \sim 5.5V, V_{IN}=V_{CC}-2.1V$		1.4	2.4	mA	
Input Capacitance	C_I	$V_{CC}=4.5V \sim 5.5V, V_{IN}=V_{CC}$ or GND		3	10	pF	

■ SWITCHING CHARACTERISTICS ($C_L=50pF, T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (CLR) to output (Q or Q̄)	t_{PLH} / t_{PHL}	$V_{CC}=4.5V$		21	35	ns
		$V_{CC}=5.5V$		17	31	ns
Propagation delay from input (CLK) to output (Q or Q̄)	t_{PLH} / t_{PHL}	$V_{CC}=4.5V$		20	28	ns
		$V_{CC}=5.5V$		18	25	ns

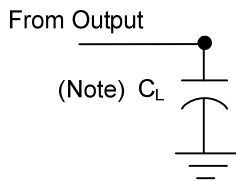
■ TIMING REQUIREMENTS (Input: $t_R, t_F \leq 2.5\text{ns}$; $\text{PRR} \leq 1\text{MHz}$)

PARAMETER	SYMBOL	Conditions	MIN	TYP	MAX	UNIT
Clock frequency	f_{CLOCK}	$V_{\text{CC}}=4.5\text{V}$			27	MHZ
		$V_{\text{CC}}=5.5\text{V}$			30	MHZ
Pulse duration	t_W	$V_{\text{CC}}=4.5\text{V}$	18			ns
		$V_{\text{CC}}=5.5\text{V}$	16			ns
Setup time before CLK↓	t_{SU}	$V_{\text{CC}}=4.5\text{V}$	12			ns
		$V_{\text{CC}}=5.5\text{V}$	11			ns
Hold time ,data after CLK↓	t_{H}	$V_{\text{CC}}=4.5\text{V}$	0			ns
		$V_{\text{CC}}=5.5\text{V}$	0			ns

■ OPERATING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load.		35		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance. $C_L=50\text{pF}$, $R_L=1\text{K}\Omega$.

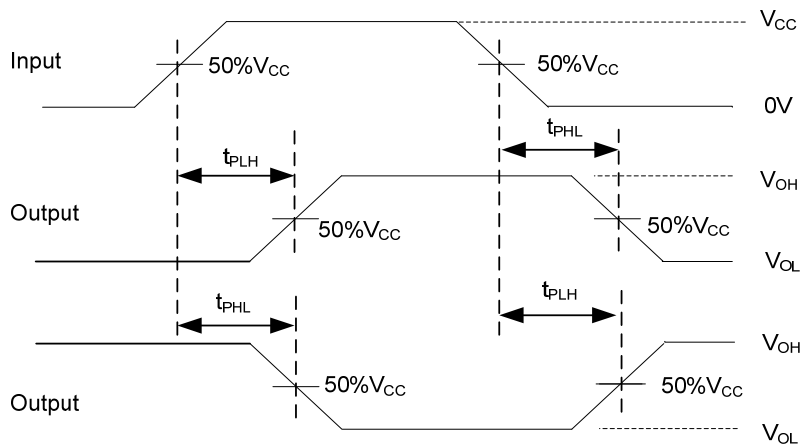


Fig 1. Load circuitry for switching times

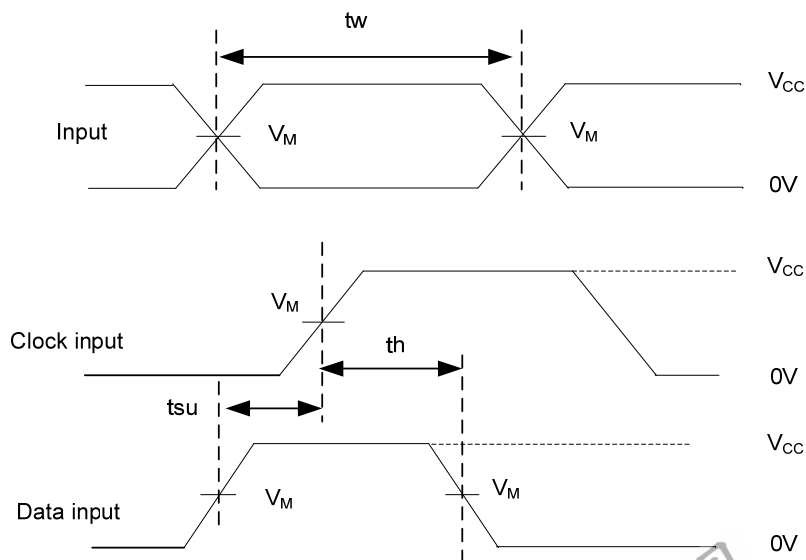


Fig 2. Propagation delay from input to output and input voltage waveforms.

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10\text{MHz}$, $Z_O = 50\Omega$.

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