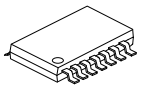
U74LCX74

CMOS IC

LOW VOLTAGE DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH 5V TOLERANT INPUTS



TSSOP-14

■ DESCRIPTION

The **U74LCX74** is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ high

■ FEATURES

* 2.3V-3.6V V_{CC} specifications provided
* 5V tolerant inputs
* 7.0 ns t_{PD} max (V_{CC}=3.3V), I_{CC}=10μA (max.)
* Power down high impedance inputs and outputs
* ±24mA output drive (V_{CC}=3.0V)

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LCX74L-P14-R	U74LCX74G-P14-R	TSSOP-14	Tape Reel

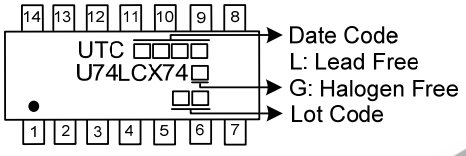
U74LCX74G-P14-R

(1)Packing Type — (1) R: Tape Reel

(2)Package Type — (2) P14: TSSOP-14

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

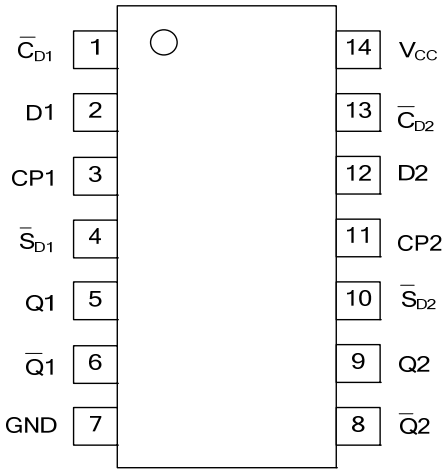
■ MARKING



FLYING 汎翊國際有限公司 www.flying1688.com

Copyright © 2014 Unisonic Technologies Co., Ltd

■ PIN CONFIGURATION



■ PIN DESCRIPTIONS

Pin Names	Description
D1, D2	Data inputs
CP1, CP2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q1, $\overline{Q}_1$, Q2, $\overline{Q}_2$	Outputs

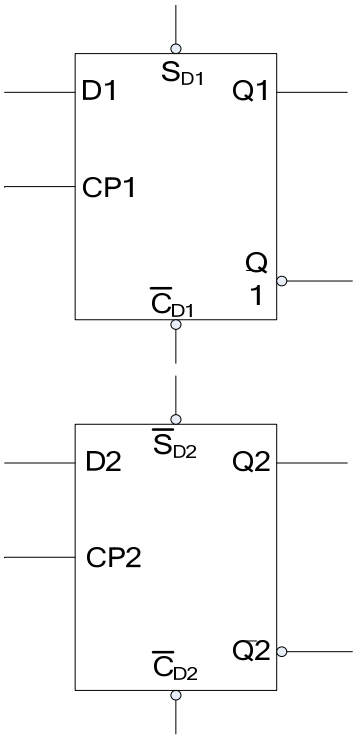
■ FUNCTION TABLE (each gate)

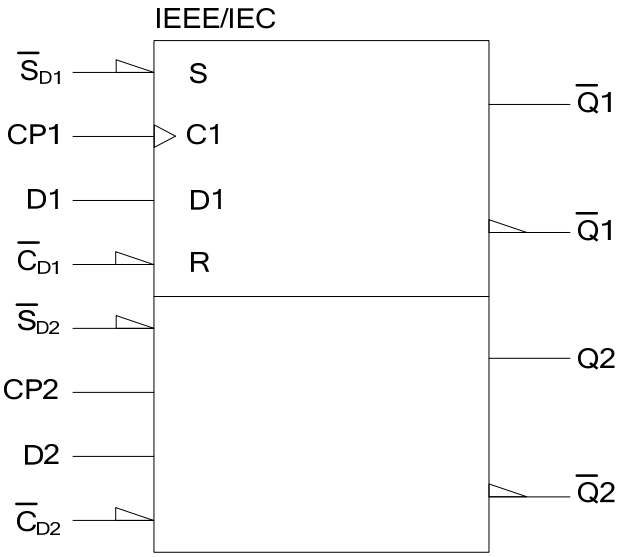
INPUT				OUTPUT		Function
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	H	H	L	Load and Read Register
H	H	↑	L	L	H	
H	H	L	X	Q_0	$\overline{Q}_0$	Hold

H=High Voltage Level; L=Low Voltage Level;
X=Immaterial; ↑=Low-to-High Clock Transition;
Q_0 ($\overline{Q}_0$)=Previous Q($\overline{Q}$) before Low-to-High Transition of Clock

FLYING 汎翊國際有限公司 www.flying1688.com

■ LOGIC DIAGRAM (positive logic)





汎翊國際有限公司
www.flying1688.com
FLYING

■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7.0	V
Input Voltage	V_{IN}	-0.5~ 7.0	V
Output Voltage	V_{OUT}	-0.5~V_{CC}+0.5	V
Input Diode Current(V_I<GND)	I_{IK}	-50	mA
Output Diode Current(V_O<GND or V_O>V_{CC})	I_{OK}	±50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Ground Current	I_{GND}	±100	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0		3.6	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	Input Edge Rate, V_{IN}=0.8V-2V, V_{CC}=3v	0		10	ns/V
Operating Temperature	T_A		-40		+85	°C

■ STATIC CHARACTERISTICS (T_A=-40°C to +85°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	V_{IH}	V_{CC}=2.3V to 2.7V	1.7			V
		V_{CC} =2.7V to 3.6V	2.0			
Low-level input voltage	V_{IL}	V_{CC}=2.3V to 2.7V			0.7	V
		V_{CC} =2.7V to 3.6V			0.8	
High-Level Output Voltage	V_{OH}	V_{CC}=2.3V to 3.6V, I_{OH}=-100μA	V_{CC}-0.2			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.8			
		V_{CC}=2.7V, I_{OH}=-12mA	2.2			
		V_{CC}=3V, I_{OH}=-18mA	2.4			
		V_{CC}=3V, I_{OH}=-24mA	2.2			
Low-Level Output Voltage	V_{OL}	V_{CC}=2.3V to 3.6V, I_{OL}=100uA			0.2	V
		V_{CC}=2.3V, I_{OL}=8mA			0.6	
		V_{CC}=2.7V, I_{OL}=12mA			0.4	
		V_{CC}=3V, I_{OL}=16mA			0.4	
		V_{CC}=3V, I_{OL}=24mA			0.55	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC} =2.3V ~ 3.6V, V_{IN}=0 ~ 5.5V			±5	μA
Quiescent Supply Current	I_Q	V_{CC} = 2.3V to 3.6V, V_{IN}= V_{CC} or GND			10	μA
		V_{CC} = 2.3V to 3.6V, 3.6V≤V_{IN}≤5.5V			±10	
Increase I_{CC} per input	ΔI_Q	V_{CC}=2.3V to 3.6V, V_{IH}=V_{CC}-0.6V			500	μA
Power-Off Leakage Current	I_{OFF}	V_{CC}=0, V_{IN} or V_{OUT} = 5.5V			10	μA
Input Capacitance	C_{IN}	V_{CC}=Open, V_I=0 or V_{CC}		7.0		pF
Output Capacitance	C_{OUT}	V_{CC}=3.3V, V_I=0 or V_{CC}		8.0		pF

FLYING 汎翊國際有限公司 www.flying1688.com

■ DYNAMIC CHARACTERISTICS (Input: t_r, t_f =3ns, f=1MHz, T_A= -40°C to 85°C, R_L=500Ω)

PARAMETER	SYMBOL	Conditions	MIN	TYP	MAX	UNIT
Maximum Clock Frequency	f_{MAX}	V_{CC}=2.5V±0.2V, C_L=30pF	150			MHZ
		V_{CC}=2.7V, C_L=50pF	150			
		V_{CC}=3.3V±0.3V, C_L=50pF	150			
Propagation Delay CPn to Qn or $\overline{Q}$n	t_{PHL}/t_{PLH}	V_{CC}=2.5V±0.2V, C_L=30pF	1.5		8.4	ns
		V_{CC}=2.7V, C_L=50pF	1.5		8.0	
		V_{CC}=3.3V±0.3V, C_L=50pF	1.5		7.0	
Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Qn or $\overline{Q}$n	t_{PHL}/t_{PLH}	V_{CC}=2.5V±0.2V, C_L=30pF	1.5		8.4	ns
		V_{CC}=2.7V, C_L=50pF	1.5		8.0	
		V_{CC}=3.3V±0.3V, C_L=50pF	1.5		7.0	
Setup Time	t_S	V_{CC}=2.5V±0.2V, C_L=30pF	4.0			ns
		V_{CC}=2.7V, C_L=50pF	2.5			
		V_{CC}=3.3V±0.3V, C_L=50pF	2.5			
Hold Time	t_H	V_{CC}=2.5V±0.2V, C_L=30pF	2.0			ns
		V_{CC}=2.7V, C_L=50pF	1.5			
		V_{CC}=3.3V±0.3V, C_L=50pF	1.5			
Pulse Width CP	t_W	V_{CC}=2.5V±0.2V, C_L=30pF	4.0			ns
		V_{CC}=2.7V, C_L=50pF	3.3			
		V_{CC}=3.3V±0.3V, C_L=50pF	3.3			
Pulse Width and $\overline{C}_{Dn}$, $\overline{S}_{Dn}$	t_W	V_{CC}=2.5V±0.2V, C_L=30pF	4.0			ns
		V_{CC}=2.7V, C_L=50pF	3.6			
		V_{CC}=3.3V±0.3V, C_L=50pF	3.3			

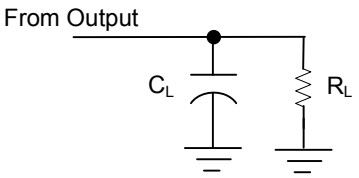
See Fig. 1 and Fig. 2 for test circuit and waveforms.

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=3.3V, V_I=0V or V_{CC}, f=10MHz		25		pF

FLYING 汎翊國際有限公司 www.flying1688.com

■ TEST CIRCUIT AND WAVEFORMS

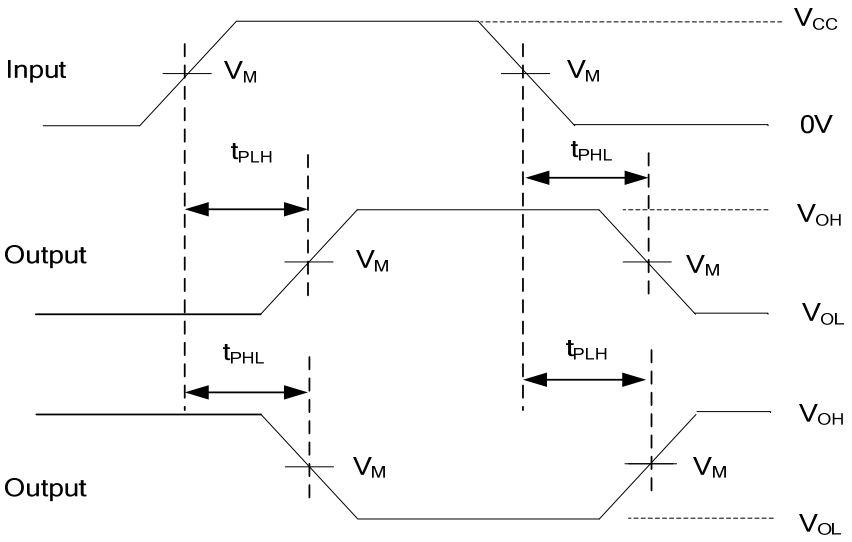


TEST CIRCUIT

Note: C_L includes probe and jig capacitance.

Fig. 1 Load circuitry for switching times.

V_{CC}	V_M	C_L	R_L
2.5V±0.2V	$V_{CC}/2$	30pF	500Ω
2.7V	1.5V	50pF	500Ω
3.3V±0.3V	1.5V	50pF	500Ω



PROPAGATION DELAY TIMES

FLYING 汎翊國際有限公司 www.flying1688.com

■ TEST CIRCUIT AND WAVEFORMS(Cont.)

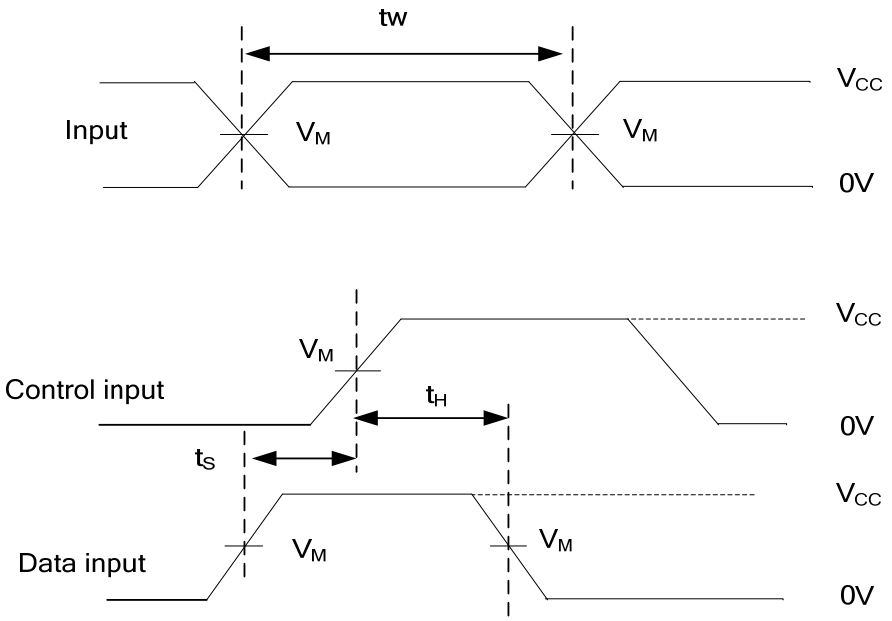


Fig. 2 Propagation delay from input to output and input voltage waveforms.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.