

# U74LVC06A

CMOS IC

## HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

### ■ DESCRIPTION

The **U74LVC06A** contain six independent inverter buffers/drivers with open drain outputs, and performs the Boolean function  $Y = \bar{A}$  in positive logic.

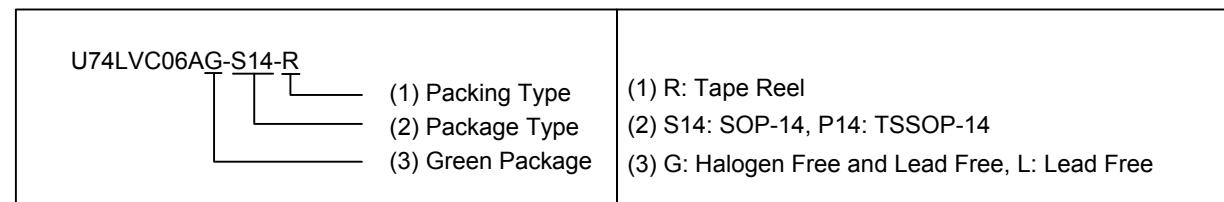
This device has power-down protective circuit preventing destruction of the device when it is powered down.

### ■ FEATURES

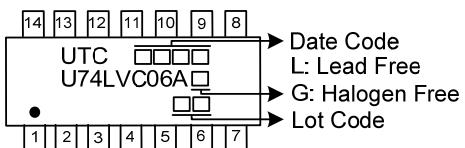
- \* Operate From 1.65V to 3.6V
- \* Inputs and Open-Drain Outputs Accept Voltages to 5.5V
- \*  $I_{OFF}$  Supports Partial-Power-Down Mode
- \* Low Power Dissipation

### ■ ORDERING INFORMATION

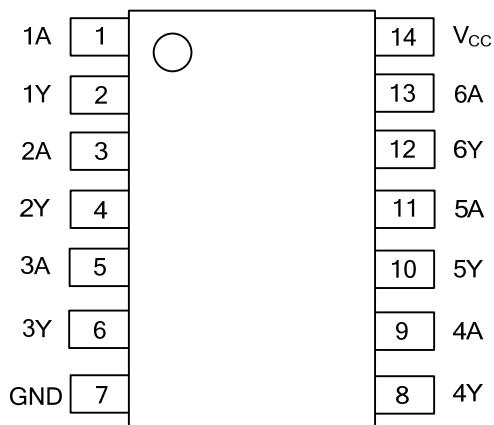
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC06AL-S14-R	U74LVC06AG-S14-R	SOP-14	Tape Reel
U74LVC06AL-P14-R	U74LVC06AG-P14-R	TSSOP-14	Tape Reel



### ■ MARKING



### ■ PIN CONFIGURATION

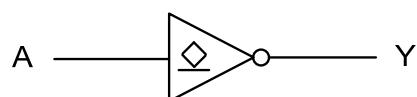


### ■ FUNCTION TABLE (Each Inverter)

INPUT(A)	OUTPUT(Y)
H	L
L	H

Note: H: HIGH voltage level; L: LOW voltage level.

### ■ LOGIC DIAGRAM (Each Inverter)



Logic Symbol

### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5 ~ +6.5	V
Input Voltage	$V_{IN}$	-0.5 ~ +6.5	V
Output Voltage	$V_{OUT}$	-0.5 ~ +6.5	V
$V_{CC}$ or GND Current	$I_{CC}$	$\pm 100$	mA
Continuous Output Current ( $V_{OUT}=0$ to $V_{CC}$ )	$I_{OUT}$	$\pm 50$	mA
Input Clamp Current ( $V_{IN}<0$ )	$I_{IK}$	-50	mA
Output Clamp Current ( $V_{OUT}<0$ )	$I_{OK}$	-50	mA
Storage Temperature	$T_{STG}$	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-14	86	°C/W
	TSSOP-14	113	°C/W

### ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	Operating	1.65		3.6	V
		Data retention only	1.5			V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$		0		5.5	V
Operating Temperature	$T_A$		-40		+85	°C
Low-Level Output Current	$I_{OL}$	$V_{CC}=1.65V$			4	mA
		$V_{CC}=2.3V$			8	mA
		$V_{CC}=2.7V$			12	mA
		$V_{CC}=3V$			24	mA

### ■ ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	$V_{IH}$	$V_{CC}=1.65V \sim 1.95V$	0.65x $V_{CC}$			V
		$V_{CC}=2.3V \sim 2.7V$	1.7			V
		$V_{CC}=2.7V \sim 3.6V$	2			V
Low-Level Input Voltage	$V_{IL}$	$V_{CC}=1.65V \sim 1.95V$			0.35x $V_{CC}$	V
		$V_{CC}=2.3V \sim 2.7V$			0.7	V
		$V_{CC}=2.7V \sim 3.6V$			0.8	V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=1.65 \sim 3.6V, I_{OL}=100\mu A$			0.2	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.7	V
		$V_{CC}=2.7V, I_{OL}=12mA$			0.4	V
		$V_{CC}=3.0V, I_{OL}=24mA$			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=5.5V$ or GND, $V_{CC}=3.6V$			$\pm 1$	$\mu A$
Power OFF Leakage Current	$I_{OFF}$	$V_{IN}$ or $V_{OUT}=5.5V$ , $V_{CC}=0V$			$\pm 1$	$\mu A$
Quiescent Supply Current	$I_Q$	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$ , $V_{CC}=3.6V$			1	$\mu A$
Additional Quiescent Supply Current Per Input Pin	$\Delta I_Q$	$V_{CC}=2.7 \sim 3.6V$ , One input at $V_{CC}-0.6V$ , $I_{OUT}=0$ , Other inputs at $V_{CC}$ or GND			500	$\mu A$
Input Capacitance	$C_{IN}$	$V_{IN}=V_{CC}$ or GND, $V_{CC}=3.3V$		5		pF

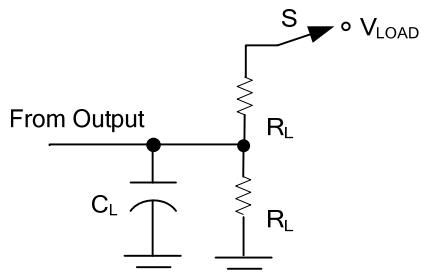
■ SWITCHING CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (nA) to output(nY)	$t_{PLZ} / t_{PZL}$	$V_{CC}=1.8\pm0.15V$ , $R_L=1K\Omega$	$C_L=30pF$	1.4		5.1	ns
		$V_{CC}=2.5\pm0.2V$ , $R_L=500\Omega$		1.0		2.8	ns
		$V_{CC}=2.7V$ , $R_L=500\Omega$	$C_L=50pF$	1.0		3.7	ns
		$V_{CC}=3.3\pm0.3V$ , $R_L=500\Omega$		1.0		3.5	ns

■ OPERATING CHARACTERISTICS ( $f=10MHz$ ,  $T_A=25^\circ C$ , unless otherwise specified)

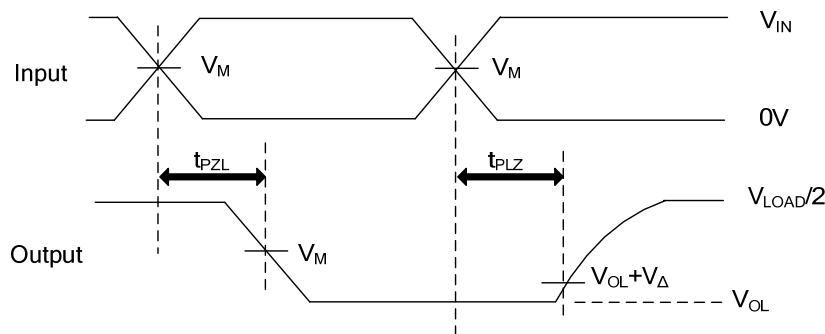
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Dissipation Capacitance Per Inverter	$C_{PD}$	$V_{CC}=1.8\pm0.15V$			2.1		pF
		$V_{CC}=2.5\pm0.2V$			2.3		pF
		$V_{CC}=3.3\pm0.3V$			2.5		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V <sub>CC</sub>	INPUTS		V <sub>M</sub>	V <sub>LOAD</sub>	V <sub>Δ</sub>	C <sub>L</sub>	R <sub>L</sub>
	V <sub>IN</sub>	t <sub>R</sub> , t <sub>F</sub>					
1.8V±0.15V	V <sub>CC</sub>	≤2ns	V <sub>CC</sub> /2	2 x V <sub>CC</sub>	0.15V	30pF	1KΩ
2.5V±0.2V	V <sub>CC</sub>	≤2ns	V <sub>CC</sub> /2	2 x V <sub>CC</sub>	0.15V	30pF	500Ω
2.7V	2.7V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω
3.3V±0.3V	2.7V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω



ENABLE AND DISABLE TIMES

Note: C<sub>L</sub> includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z<sub>O</sub> = 50Ω.

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