U74LVC563 cmos ic

# OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

#### ■ DESCRIPTION

The **U74LVC563** is a octal transparent D-TYPE latches with 3-state outputs. When the latch-enable (LE) is high, the  $\overline{Q}$  outputs follow the complements of the D inputs. When LE is low, the  $\overline{Q}$  outputs are latched at the inverses of the levels set up at the D inputs.

When the output-enable ( $\overline{OE}$ ) input is high, the  $\overline{Q}$  outputs are in a high-impedance state, and the outputs neither load nor drive the bus lines. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components. While the outputs are in the high-impedance state, old data can be retained or new data can be entered, i.e.  $\overline{OE}$  does not affect the internal operations of the latches. When  $\overline{OE}$  is low, the  $\overline{Q}$  outputs are in a normal logic state (high or low levels).

The **U74LVC563** is designed for 1.65V to 3.6V operation. Inputs can be driven from either 3.3V or 5V devices, so the U74LVC563 can be used in a mixed 3.3V/5V system environment.

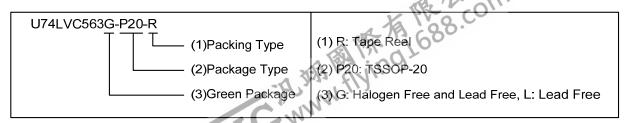
To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



- \* Wide supply voltage range from 1.65V to 3.6V
- \* Max  $t_{PD}$  of 6.8 ns from D to  $\overline{Q}$  at 3.3V
- \* Max  $t_{PD}$  of 7.6 ns from LE to  $\overline{Q}$  at 3.3V
- \* Up to 5.5V inputs accept voltages
- \* Low power consumption,  $I_{CC}$  = 10 $\mu$ A (Max.) at 3.6V
- \* ±24mA output driver at 3V
- \* I<sub>OFF</sub> supports partial-power-down mode operation

#### **■** ORDERING INFORMATION

Ordering	Dookogo	Dooking	
Lead Free Halogen Free		Package	Packing
U74LVC563L-P20-R	U74LVC563G-P20-R	TSSOP-20	Tape Reel

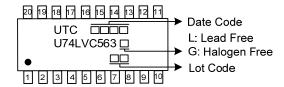


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## MARKING



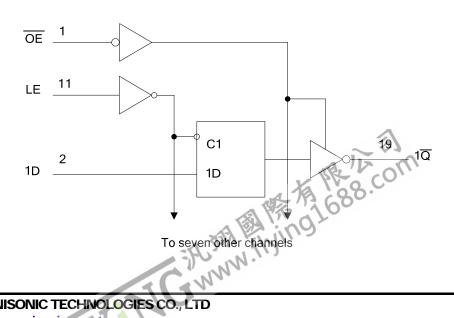
## **■ PIN CONFIGURATION**

ŌĒ [	1 0	20 V <sub>CC</sub>
1D [	2	19 1Q
2D [	3	18 2Q
3D [	4	17 3Q
4D [	5	16 4Q
5D [	6	15 5Q
6D [	7	14 6Q
7D [	8	13 7Q
8D [	9	12 8Q
GND [	10	11 LE

## **■ FUNCTION TABLE** (each latch)

INPUTS			OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	L
L	Н	L	Н
L	L	×	$\overline{Q_{o}}$
Н	X	X	Z

## ■ LOGIC DIAGRAM (positive logic)



## ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	Vcc	-0.5 ~ 6.5	V
Input Voltage	V <sub>IN</sub>	-0.5 ~ 6.5	V
Output Voltage (any output in the high-impedance or power-off state)	V <sub>OUT</sub>	-0.5 ~ 6.5	V
Output Voltage (any output in the high or low state)	V <sub>out</sub>	-0.5 ~ V <sub>CC</sub> +0.5	V
Input Clamp Current	I <sub>IK</sub>	-50	mA
Output Clamp Current	lok	-50	mA
Output Current	I <sub>OUT</sub>	±50	mA
V <sub>CC</sub> or GND Current	I <sub>CC</sub>	±100	mA
Storage Temperature	T <sub>STG</sub>	-65 ~ <b>+</b> 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT	
Supply Voltage		Operating	1.65	3.6	V	
Supply Voltage	V <sub>cc</sub>	Data retention only	1.5		V	
		$V_{CC} = 1.65V \text{ to } 1.95V$	0.65* V <sub>CC</sub>			
High-Level Input Voltage	$V_{IH}$	$V_{CC} = 2.3V \text{ to } 2.7V$	1.7		V	
		$V_{CC} = 2.7V \text{ to } 3.6V$	2			
		$V_{CC} = 1.65V \text{ to } 1.95V$		0.35* V <sub>CC</sub>		
Low-Level Input Voltage	$V_{IL}$	$V_{CC} = 2.3V \text{ to } 2.7V$		0.7	V	
		$V_{CC} = 2.7V \text{ to } 3.6V$		0.8	1	
Input Voltage	V <sub>IN</sub>		0	5.5	V	
Output Valtage	.,	High or low state	0	V <sub>CC</sub>	V	
Output Voltage	V <sub>OUT</sub>	3 state	0	5.5	V	
		V <sub>CC</sub> =1.65V		-4		
Himb Lovel Oversit Commont		V <sub>CC</sub> =2.3V		-8	mA	
High-Level Output Current	I <sub>OH</sub>	V <sub>CC</sub> =2.7V		-12		
		V <sub>CC</sub> =3V		-24		
		V <sub>CC</sub> =1.65V		4		
Lavel aval Ovitavit Commant		V <sub>CC</sub> =2.3V		8	^	
Low-Level Output Current	I <sub>OL</sub>	V <sub>CC</sub> =2.7V		12	mA	
		V <sub>CC</sub> =3V		24		
Input Transition Rise or Fall Rate	Δt/Δν		0	10	ns/V	
Operating Temperature	TA		-40	85	°C	



<sup>2.</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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# **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		$I_{OH}$ = -100 $\mu$ A, $V_{CC}$ = 1.65 $V$ to 3.6 $V$	V <sub>CC</sub> -0.2			
		$I_{OH} = -4mA, V_{CC} = 1.65V$	1.2			
High Loyal Output Valtage	W	$I_{OH} = -8mA, V_{CC} = 2.3V$	1.7			V
High-Level Output Voltage	V <sub>OH</sub>	$I_{OH} = -12 \text{mA}, V_{CC} = 2.7 \text{V}$	2.2			V
		$I_{OH} = -12 \text{mA}, V_{CC} = 3 \text{V}$	2.4			
		I <sub>OH</sub> = -24mA, V <sub>CC</sub> = 3V	2.2			
		$I_{OL} = 100 \mu A$ , $V_{CC} = 1.65 V$ to 3.6 V			0.2	
		I <sub>OL</sub> = 4mA, V <sub>CC</sub> = 1.65V			0.45	
Low-Level Output Voltage		$I_{OL} = 8mA, V_{CC} = 2.3V$			0.7	V
		$I_{OL} = 12 \text{mA}, V_{CC} = 2.7 \text{V}$			0.4	
		I <sub>OL</sub> = 24mA, V <sub>CC</sub> = 3V			0.55	
Input Leakage Current		N - 0 to 5 5 /				
(D, LE, or OE inputs)	I <sub>I(LEAK)</sub>	$V_{IN} = 0$ to 5.5V, $V_{CC} = 3.6V$			±5	μA
OFF-state Current	l <sub>OFF</sub>	$V_{IN}$ or $V_{O} = 5.5V$ , $V_{CC} = 0V$			±10	μΑ
High-impedance state Current	l <sub>oz</sub>	$V_{\rm O}$ = 0 to 5.5V, $V_{\rm CC}$ = 3.6V			±10	μΑ
Ouiogoopt Supply Current		$I_{OUT} = 0$ , $V_{IN} = V_{CC}$ or GND,			10	
Quiescent Supply Current	I <sub>CC</sub>	$V_{CC}$ =3.6 $V_{IN}$ =3.6 $V$ to 5.5 $V$ ,in disabled state			10	μA
Additional quiescent Supply	A 1	One input at $V_{CC}$ -0.6V, $V_{CC}$ =2.7V to 3.6V,			500	
Current	Δ l <sub>CC</sub>	other inputs at V <sub>CC</sub> or GND			500	μA
Input Capacitance	C <sub>IN</sub>	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3V$ (Note 1)		4		pF
Output Capacitance	Соит	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.3V$ (Note 1)		5.5		pF

Note: 1. All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25 °C.

## **TIMING REQUIREMENTS** (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	
Dulas duration I E high		$V_{CC} = 2.7V$	3.3			
Pulse duration, LE high	t <sub>W</sub>	$V_{CC} = 3.3V \pm 0.3V$	3.3		ns	
Octors times and the before LEL		V <sub>CC</sub> = 2.7V	2		ns	
Setup time, data before LE↓	t <sub>SU</sub>	V <sub>CC</sub> = 3.3V±0.3V	2			
Light time data after LT		V <sub>CC</sub> = 2.7V	1.5			
Hold time, data after LE↓	Īμ	$V_{CC} = 3.3V \pm 0.3V$	1.5		ns	

## **SWITCHING CHARACTERISTICS** (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	
Propagation delay	t <sub>PLH</sub> /t <sub>PHL</sub>	$V_{CC}$ =2.7V, $C_L$ =50pF, $R_L$ =500 $\Omega$		7.8		
from input D to output Q	(t <sub>PD</sub> )	$V_{CC}$ =3.3±0.3V, $C_L$ =50pF, $R_L$ =500 $\Omega$	1.5	6.8	ns	
Propagation delay	t <sub>PLH</sub> /t <sub>PHL</sub>	$V_{CC}$ =2.7V, $C_L$ =50pF, $R_L$ =500 $\Omega$		8.2		
from input LE to output $\overline{Q}$	(t <sub>PD</sub> )	$V_{CC}$ =3.3±0.3V, $C_L$ =50pF, $R_L$ =500 $\Omega$	2	7.6	ns	
Propagation delay	t <sub>PZL</sub> /t <sub>PZH</sub>	$V_{CC}$ =2.7V, $C_L$ =50pF, $R_L$ =500 $\Omega$		8.7		
from input $\overline{OE}$ to output $\overline{Q}$	(t <sub>EN</sub> )	$V_{CC}$ =3.3±0.3V, $C_L$ =50pF, $R_L$ =500 $\Omega$	1.5	7.7	ns	
Propagation delay	t <sub>PLZ</sub> /t <sub>PHZ</sub>	$V_{CC}$ =2.7V, $C_L$ =50pF, $R_L$ =500 $\Omega$		7.6		
from input $\overline{OE}$ to output $\overline{Q}$	(t <sub>DIS</sub> )	$V_{CC}$ =3.3±0.3V, $C_L$ =50pF, $R_L$ =500 $\Omega$	1.5	7	ns	
■ OPERATING CHARACTERISTICS (T <sub>A</sub> =25°C)						

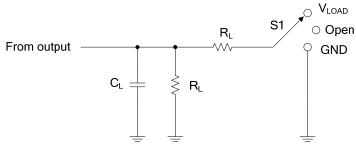
# **OPERATING CHARACTERISTICS** (T<sub>A</sub> =25°C)

			37.07			
	PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT	
	Power Dissipation Capacitance	C	OE = 0, f=10MHz, outputs enabled	46	_ ne	
	Capacitance	$C_{PD}$	OE = 1, f=10MHz, outputs disabled	3	pF	
OZ NWW. FIVINGUS CISCUSCO						
	UNISONIC TECHNOLOGIES CO., LTD					



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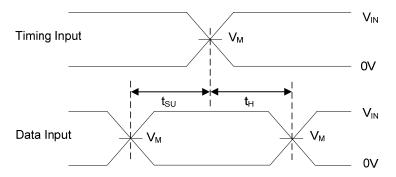
#### **TEST CIRCUIT AND WAVEFORMS**



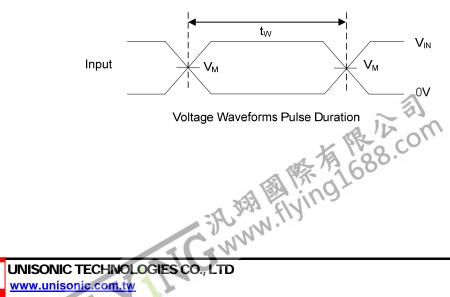
Test Circuit

TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	$V_{LOAD}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

\/	Inputs		V	V	0	Rı	
V <sub>CC</sub>	$V_{IN}$	t <sub>R</sub> , t <sub>F</sub>	$V_{M}$	V <sub>LOAD</sub>	CL	ΚL	VΔ
2.7V	V <sub>CC</sub>	≤2.5ns	1.5V	6V	50pF	500Ω	
3.3V±0.3V	V <sub>CC</sub>	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V

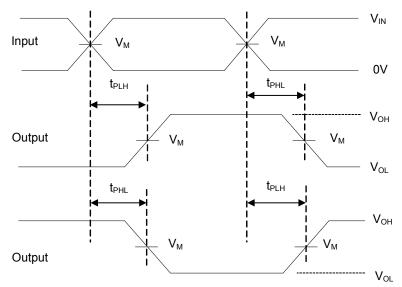


Voltage Waveforms Setup and Hold Times

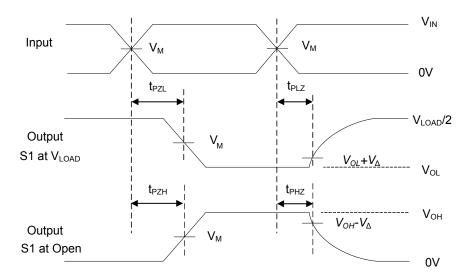


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## ■ TEST CIRCUIT AND WAVEFORMS (Cont.)



**Voltage Waveforms Propagation Delay Times** 



**Voltage Waveforms Enable and Disable Times** 

Notes: 1. C<sub>L</sub> includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics:  $P_{RR} \le 10 \text{MHz}$ ,  $Z_0 = 50 \Omega$ .

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