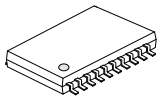
U74LVC563

CMOS IC

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



TSSOP-20

■ DESCRIPTION

The **U74LVC563** is a octal transparent D-TYPE latches with 3-state outputs. When the latch-enable (LE) is high, the $\overline{Q}$ outputs follow the complements of the D inputs. When LE is low, the $\overline{Q}$ outputs are latched at the inverses of the levels set up at the D inputs.

When the output-enable ($\overline{OE}$) input is high, the $\overline{Q}$ outputs are in a high-impedance state, and the outputs neither load nor drive the bus lines. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components. While the outputs are in the high-impedance state, old data can be retained or new data can be entered, i.e. $\overline{OE}$ does not affect the internal operations of the latches. When $\overline{OE}$ is low, the $\overline{Q}$ outputs are in a normal logic state (high or low levels).

The **U74LVC563** is designed for 1.65V to 3.6V operation. Inputs can be driven from either 3.3V or 5V devices, so the U74LVC563 can be used in a mixed 3.3V/5V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* Wide supply voltage range from 1.65V to 3.6V
* Max t_{PD} of 6.8 ns from D to $\overline{Q}$ at 3.3V
* Max t_{PD} of 7.6 ns from LE to $\overline{Q}$ at 3.3V
* Up to 5.5V inputs accept voltages
* Low power consumption, I_{CC} = 10μA (Max.) at 3.6V
* ±24mA output driver at 3V
* I_{OFF} supports partial-power-down mode operation

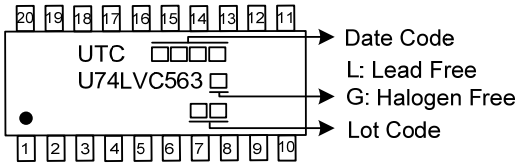
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC563L-P20-R	U74LVC563G-P20-R	TSSOP-20	Tape Reel

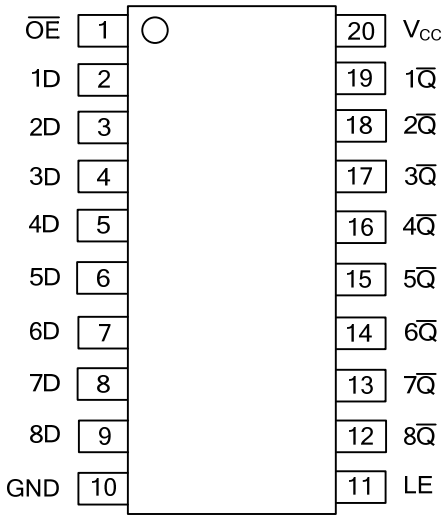
U74LVC563G-P20-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) P20: TSSOP-20
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



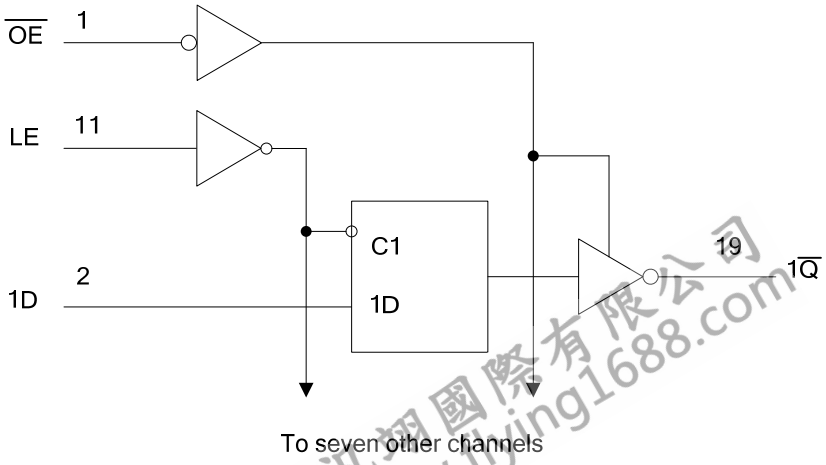
■ PIN CONFIGURATION



■ FUNCTION TABLE (each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q_0}$
H	X	X	Z

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 6.5	V
Input Voltage	V_{IN}	-0.5 ~ 6.5	V
Output Voltage (any output in the high-impedance or power-off state)	V_{OUT}	-0.5 ~ 6.5	V
Output Voltage (any output in the high or low state)	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Clamp Current	I_{IK}	-50	mA
Output Clamp Current	I_{OK}	-50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65	3.6	V
		Data retention only	1.5		
High-Level Input Voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	0.65* V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 2.7V to 3.6V	2		
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.65V to 1.95V		0.35* V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 2.7V to 3.6V		0.8	
Input Voltage	V_{IN}		0	5.5	V
Output Voltage	V_{OUT}	High or low state	0	V_{CC}	V
		3 state	0	5.5	
High-Level Output Current	I_{OH}	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=2.7V		-12	
		V_{CC}=3V		-24	
Low-Level Output Current	I_{OL}	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=2.7V		12	
		V_{CC}=3V		24	
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$		0	10	ns/V
Operating Temperature	T_A		-40	85	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	I_{OH} = -100μA, V_{CC} = 1.65V to 3.6V	V_{CC}-0.2			V
		I_{OH} = -4mA, V_{CC} = 1.65V	1.2			
		I_{OH} = -8mA, V_{CC} = 2.3V	1.7			
		I_{OH} = -12mA, V_{CC} = 2.7V	2.2			
		I_{OH} = -12mA, V_{CC} = 3V	2.4			
		I_{OH} = -24mA, V_{CC} = 3V	2.2			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100μA, V_{CC} = 1.65V to 3.6V			0.2	V
		I_{OL} = 4mA, V_{CC} = 1.65V			0.45	
		I_{OL} = 8mA, V_{CC} = 2.3V			0.7	
		I_{OL} = 12mA, V_{CC} = 2.7V			0.4	
		I_{OL} = 24mA, V_{CC} = 3V			0.55	
Input Leakage Current (D, LE, or $\overline{OE}$ inputs)	$I_{I(LEAK)}$	V_{IN} = 0 to 5.5V, V_{CC} = 3.6V			±5	μA
OFF-state Current	I_{OFF}	V_{IN} or V_O = 5.5V, V_{CC} = 0V			±10	μA
High-impedance state Current	I_{OZ}	V_O = 0 to 5.5V, V_{CC} = 3.6V			±10	μA
Quiescent Supply Current	I_{CC}	I_{OUT} = 0, V_{CC}=3.6V; V_{IN} = V_{CC} or GND			10	μA
		I_{OUT} = 0, V_{CC}=3.6V; V_{IN}=3.6V to 5.5V,in disabled state			10	
Additional quiescent Supply Current	ΔI_{CC}	One input at V_{CC}-0.6V,V_{CC}=2.7V to 3.6V, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	V_{IN} = V_{CC} or GND, V_{CC}=3.3V (Note 1)		4		pF
Output Capacitance	C_{OUT}	V_{OUT} = V_{CC} or GND, V_{CC}=3.3V (Note 1)		5.5		pF

Note: 1. All typical values are at V_{CC} = 3.3 V, T_A = 25 °C.

■ TIMING REQUIREMENTS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Pulse duration, LE high	t_W	V_{CC} = 2.7V	3.3		ns
		V_{CC} = 3.3V±0.3V	3.3		
Setup time, data before LE↓	t_{SU}	V_{CC} = 2.7V	2		ns
		V_{CC} = 3.3V±0.3V	2		
Hold time, data after LE↓	t_H	V_{CC} = 2.7V	1.5		ns
		V_{CC} = 3.3V±0.3V	1.5		

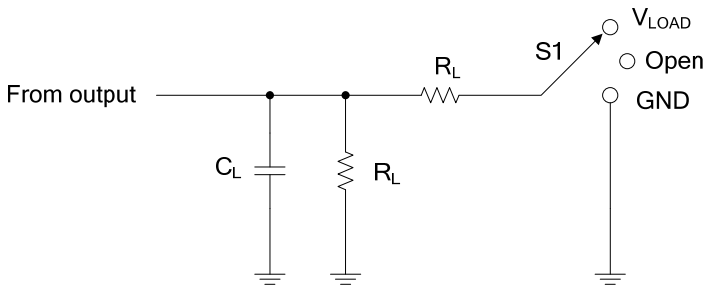
■ SWITCHING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Propagation delay from input D to output $\overline{Q}$	t_{PLH}/t_{PHL} (t_{PD})	V_{CC}=2.7V, C_L=50pF, R_L=500Ω		7.8	ns
		V_{CC}=3.3±0.3V, C_L=50pF, R_L=500Ω	1.5	6.8	
Propagation delay from input LE to output $\overline{Q}$	t_{PLH}/t_{PHL} (t_{PD})	V_{CC}=2.7V, C_L=50pF, R_L=500Ω		8.2	ns
		V_{CC}=3.3±0.3V, C_L=50pF, R_L=500Ω	2	7.6	
Propagation delay from input $\overline{OE}$ to output $\overline{Q}$	t_{PZL}/t_{PZH} (t_{EN})	V_{CC}=2.7V, C_L=50pF, R_L=500Ω		8.7	ns
		V_{CC}=3.3±0.3V, C_L=50pF, R_L=500Ω	1.5	7.7	
Propagation delay from input $\overline{OE}$ to output $\overline{Q}$	t_{PLZ}/t_{PHZ} (t_{DIS})	V_{CC}=2.7V, C_L=50pF, R_L=500Ω		7.6	ns
		V_{CC}=3.3±0.3V, C_L=50pF, R_L=500Ω	1.5	7	

■ OPERATING CHARACTERISTICS (T_A =25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power Dissipation Capacitance	C_{PD}	$\overline{OE}$ = 0, f=10MHz, outputs enabled	46	pF
		$\overline{OE}$ = 1, f=10MHz, outputs disabled	3	

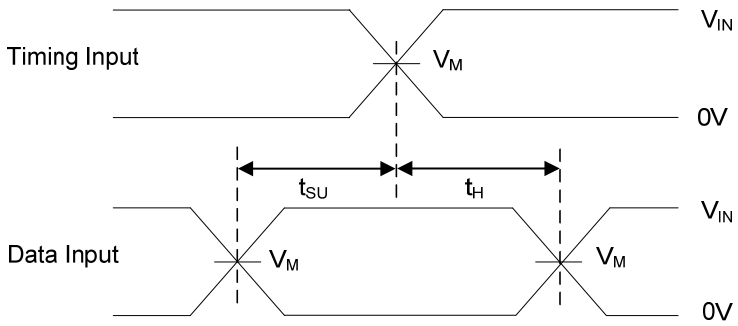
■ TEST CIRCUIT AND WAVEFORMS



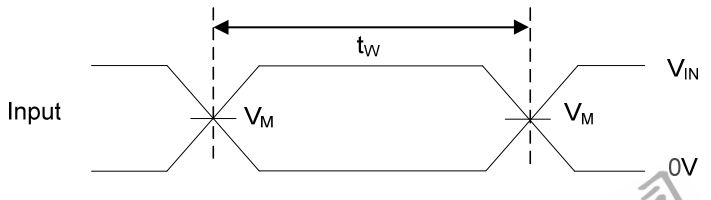
Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
2.7V	V_{CC}	≤2.5ns	1.5V	6V	50pF	500Ω	
3.3V±0.3V	V_{CC}	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V

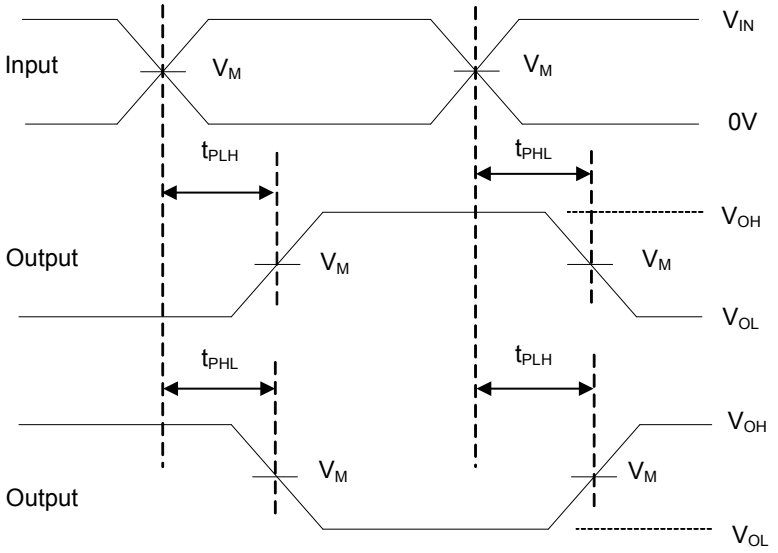


Voltage Waveforms Setup and Hold Times

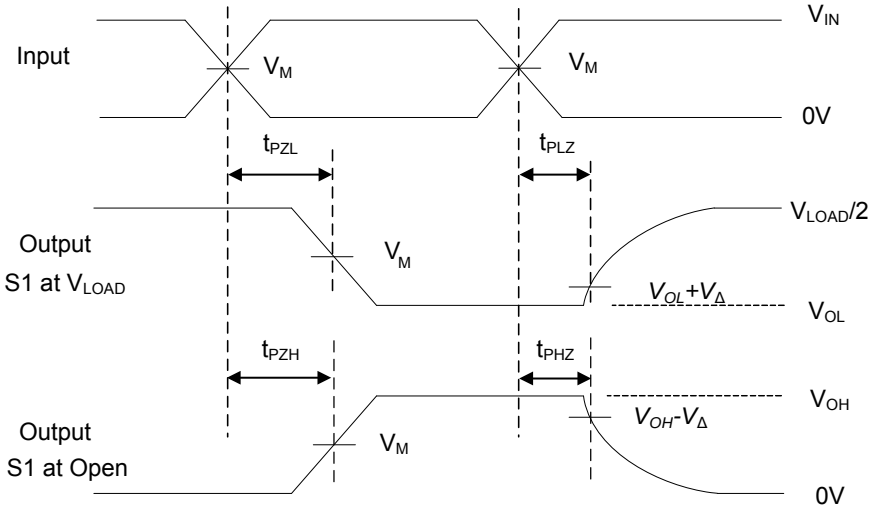


Voltage Waveforms Pulse Duration

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: P_{RR} ≤10MHz, Z_O = 50Ω.