



## UC3846

## LINEAR INTEGRATED CIRCUIT

### CURRENT MODE PWM CONTROLLER

#### DESCRIPTION

The UTC **UC3846** control IC offers all necessary features for accomplishment of fixed frequency, current mode control functions, however it contains the least external parts. The performance of this technique is superior to the others in better line regulation, enhanced load response characteristics while designing a simpler and easier control loop for design. It owns topological advantages of inherent pulse-by-pulse current limiting, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" for equal current sharing.

Protection loop includes soft start, built-in under-voltage lockout and programmable current limit. The shutdown circuitry can provide either a complete shutdown with automatic restart or the supply off-latch.

In addition, many other features can also be available, including fully latched operation, double pulse suppression, deadline adjust, and a  $\pm 1\%$  trimmed bandgap reference.

The UTC **UC3846** features low outputs in the OFF state.

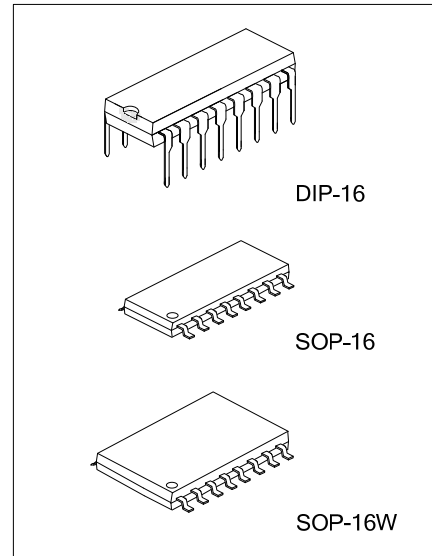
#### FEATURES

- \* Built-in under-voltage lockout
- \* Soft start
- \* Shutdown function
- \* 500kHz operation
- \* Feed forward compensation
- \*  $\pm 1\%$  bandgap reference
- \* Programmable pulse-by-pulse current limiting
- \* Improved load response characteristics
- \* Parallel operation capability for modular power systems
- \* Differential current sense amplifier with wide common mode range
- \* Double pulse suppression
- \* 500mA (Peak) totem-pole outputs
- \* Automatic symmetry correction in push-pull configuration

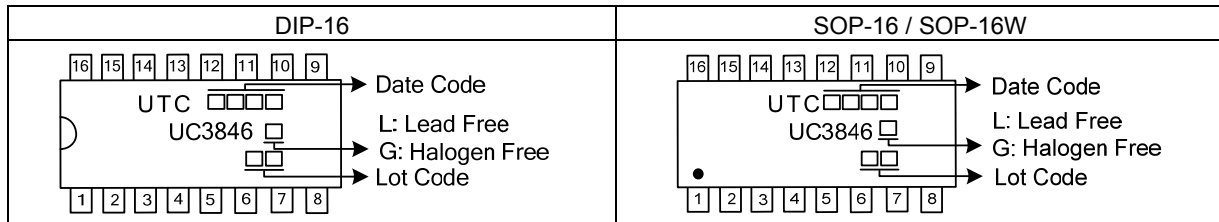
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3846L-D16-T	UC3846G-D16-T	DIP-16	Tube
UC3846L-S16-T	UC3846G-S16-T	SOP-16	Tube
UC3846L-S16-R	UC3846G-S16-R	SOP-16	Tape Reel
UC3846L-S16W-T	UC3846G-S16W-T	SOP-16W	Tube
UC3846L-S16W-R	UC3846G-S16W-R	SOP-16W	Tape Reel

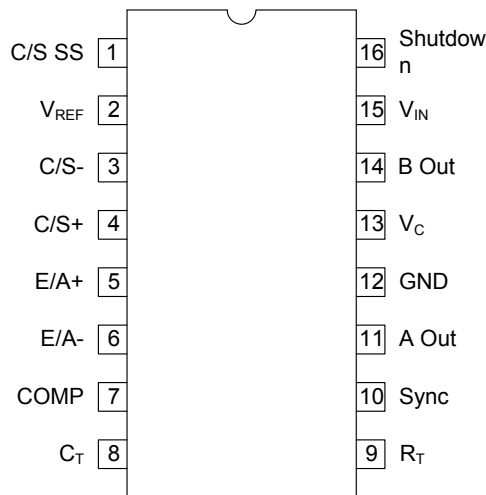
<p>UC3846G-D16-T</p>	<p>(1) T: Tube, R: Tape Reel  (2) D16: DIP-16, S16: SOP-16, S16W: SOP-16W  (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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### MARKING



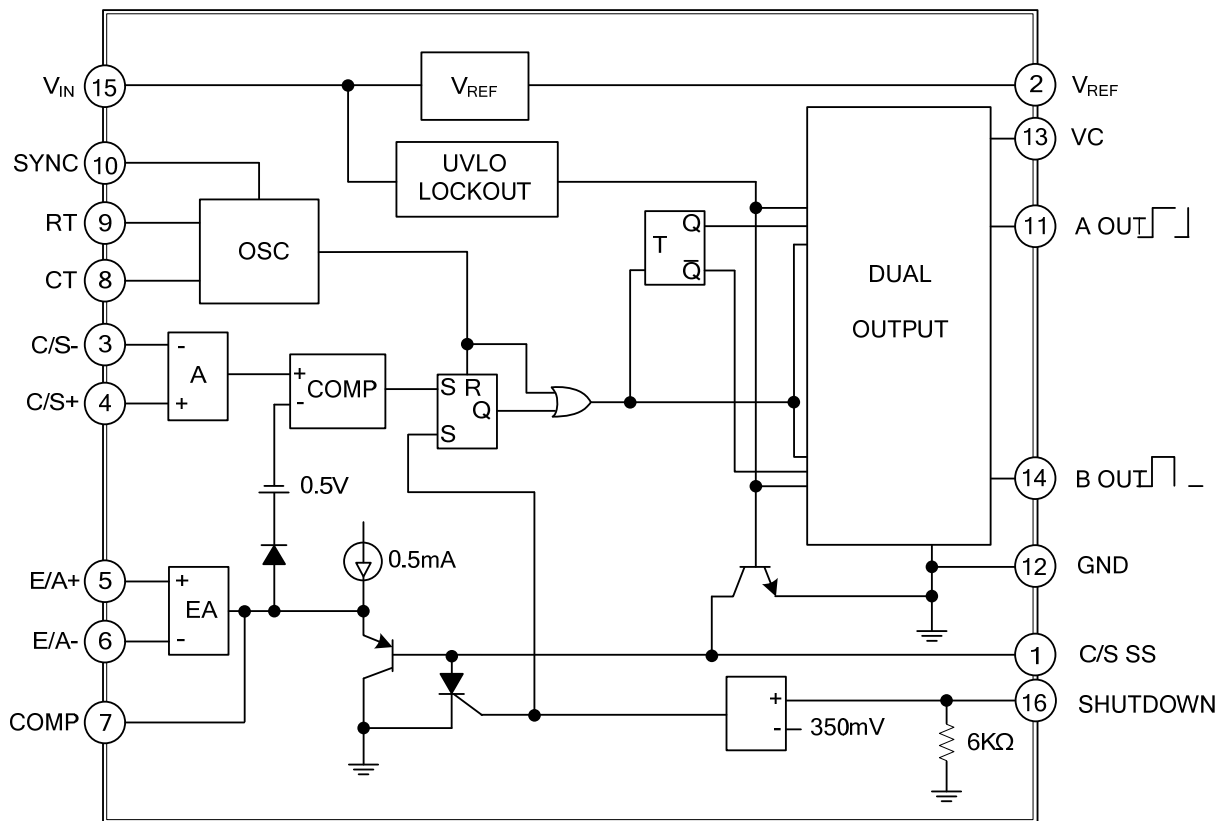
### PIN CONFIGURATION



### PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	C/S SS	Adjustment of Current Limiting
2	$V_{REF}$	Internal Reference Voltage
3	C/S-	Forward Input of Current Limiting
4	C/S+	Backward Input of Current Limiting
5	E/A+	Forward Input of Error Amplifier
6	E/A-	Backward Input of Error Amplifier
7	COMP	Output of Error Amplifier
8	$C_T$	External Capacity for Frequency
9	$R_T$	External Resistor for Frequency
10	SYNC	Synchronization for Frequency of Oscillator
11	A OUT	Dual Output A
12	GND	Ground
13	$V_C$	Power Supply of the Collector
14	B OUT	Dual Output B
15	$V_{IN}$	DC Power Supply Input
16	SHUTDOWN	Shutdown Controller

## ■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Note)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (Pin 15)	$V_{IN}$	+40	V
Collector Supply Voltage (Pin 13)	$V_C$	+40	V
Output Current, Source or Sink (Pins 11, 14)	$I_O$	500	mA
Analog Inputs (Pins 3, 4, 5, 6, 16)	$V_A$	-0.3 ~ + $V_{IN}$	V
Reference Output Current (Pin 2)	$I_{REF}$	-30	mA
Sync Output Current (Pin 10)	$I_{SYNC-OUT}$	-5	mA
Error Amplifier Output Current (Pin 7)	$I_{O-EA}$	-5	mA
Soft Start Sink Current (Pin 1)	$I_{SINK}$	50	mA
Oscillator Charging Current (Pin 9)	$I_{OSC}$	5	mA
Power Dissipation	$T_A=25^\circ\text{C}$	$P_D$	1000
	$T_C=25^\circ\text{C}$		2000
Storage Temperature	$T_{STG}$	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

( $T_J=T_A=0^\circ\text{C}\sim+70^\circ\text{C}$ ,  $V_{IN}=15\text{V}$ ,  $R_T=10\text{k}$ ,  $C_T=4.7\text{nF}$ , Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE SECTION</b>						
Output Voltage	$V_{REF}$	$T_J=25^\circ\text{C}$ , $I_O=1\text{mA}$	5.0	5.1	5.2	V
Line Regulation	$\Delta V_1$	$V_{IN}=8\text{V}\sim 40\text{V}$		5	20	mV
Load Regulation	$\Delta V_2$	$I_L=1\text{mA}\sim 10\text{mA}$		3	15	mV
Temperature Stability	$V_S$	Over Operating Range, (Note 2)		0.4		mV/ $^\circ\text{C}$
Total Output Variation	$V_{REF-O}$	Line, Load, and Temperature (Note 2)	4.95		5.25	V
Output Noise Voltage	$V_N$	$10\text{Hz}\leq f\leq 10\text{kHz}$ , $T_J=25^\circ\text{C}$ (Note 2)		100		$\mu\text{V}$
Long Term Stability	$\Delta V_3$	$T_J=125^\circ\text{C}$ , 1000 Hrs. (Note 2)		5		mV
Short Circuit Output Current	$I_S$	$V_{REF}=0\text{V}$	-10	-45		mA
<b>OSCILLATOR SECTION</b>						
Initial Accuracy	$F_{OSC}$	$T_J=25^\circ\text{C}$	39	43	47	kHz
Voltage Stability	$\Delta V$	$V_{IN}=8\text{V}\sim 40\text{V}$		-1	2	%
Temperature Stability	$\Delta T_S$	Over Operating Range (Note 2)		-1		%
Sync Output High Level	$V_{OH(SYNC)}$		3.9	4.35		V
Sync Output Low Level	$V_{OL(SYNC)}$			2.3	2.5	V
Sync Input High Level	$V_{IH(SYNC)}$	Pin 8=0V	3.9			V
Sync Input Low Level	$V_{IL(SYNC)}$	Pin 8=0V			2.5	V
Sync Input Current	$I_{SYNC}$	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5	mA
<b>ERROR AMP SECTION</b>						
Input Offset Voltage	$V_{IO}$			0.5	10	mV
Input Bias Current	$I_{BIAS}$			-0.6	-2	$\mu\text{A}$
Input Offset Current	$I_{IO}$			40	250	nA
Common Mode Range	$V_{CM}$	$V_{IN}=8\text{V}\sim 40\text{V}$	0		$V_{IN}-2\text{V}$	V
Open Loop Voltage Gain	$G_{VO}$	$\Delta V_O=1.2\sim 3\text{V}$ , $V_{CM}=2\text{V}$	80	105		dB
Unity Gain Bandwidth	B	$T_J=25^\circ\text{C}$ (Note 2)	0.7	1.0		MHz
CMRR	$CMRR_A$	$V_{CM}=0\text{V}\sim 38\text{V}$ , $V_{IN}=40\text{V}$	75	100		dB
PSRR	$PSRR_A$	$V_{IN}=8\text{V}\sim 40\text{V}$	80	105		dB
Output Sink Current	$I_{SINK}$	$V_{ID}=-15\text{mV}\sim -5\text{V}$ , $V_{PIN7}=1.2\text{V}$	2	6		mA
Output Source Current	$I_{SOURCE}$	$V_{ID}=15\text{mV}\sim 5\text{V}$ , $V_{PIN7}=2.5\text{V}$	-0.2	-0.5		mA
High Level Output Voltage	$V_{OH}$	$R_L=(\text{Pin } 7) 15\text{k}\Omega$	4.3	4.6		V
Low Level Output Voltage	$V_{OL}$		0.7	1		V

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT SENSE AMPLIFIER SECTION</b>						
Amplifier Gain	$G_A$	$V_{PIN3}=0V$ , Pin 1 Open (Note 3, 4)	2.5	2.75	3.0	V
Maximum Differential Input Signal ( $V_{PIN4}-V_{PIN3}$ )	$V_{IN(MAX)}$	Pin 1 Open (Note 3), $R_L$ (Pin 7)=15k $\Omega$	1.1	1.2		V
Input Offset Voltage	$V_{IO}$	$V_{PIN1}=0.5V$ , Pin 7 Open (Note 3)		5	25	mV
CMRR	$CMRR_A$	$V_{CM}=1V\sim 12V$	60	83		dB
PSRR	$PSRR_A$	$V_{IN}=8V\sim 40V$	60	84		dB
Input Bias Current	$I_{BIAS}$	$V_{PIN1}=0.5V$ , Pin 7 Open (Note 3)		-2.5	-10	$\mu A$
Input Offset Current	$I_{IO}$	$V_{PIN1}=0.5V$ , Pin 7 Open (Note 3)		0.08	1	$\mu A$
Input Common Mode Range	$\Delta V_R$		0		$V_{IN}-3$	V
Delay to Outputs	$t_D$	$T_J=25^\circ C$ , (Note 2)		200	500	ns
<b>CURRENT LIMIT ADJUST SECTION</b>						
Current Limit Offset	$V_L$	$V_{PIN3}=0V$ , $V_{PIN4}=0V$ , Pin 7 Open (Note 3)	0.45	0.5	0.55	V
Input Bias Current	$I_B$	$V_{PIN5}=V_{REF}$ , $V_{PIN6}=0V$		-10	-30	$\mu A$
<b>SHUTDOWN TERMINAL SECTION</b>						
Threshold Voltage	$V_{TH}$		250	350	550	mV
Input Voltage Range	$\Delta V_{SHUT}$		0		$V_{IN}$	V
Minimum Latching Current ( $I_{PIN1}$ )	$I_{LATCH}$	(Note 6)	3.0	1.5		mA
Maximum Non-Latching Current ( $I_{PIN1}$ )	$I_{NONLATCH}$	(Note 7)		1.5	0.8	mA
Delay to Outputs	$t_{D-SHUT}$	$T_J=25^\circ C$ (Note 2)		300	600	ns
<b>OUTPUT SECTION</b>						
Collector-Emitter Voltage	$V_T$		40			V
Collector Leakage Current	$I_L$	$V_C=40V$ (Note 5)			200	$\mu A$
Output Low Level	$V_{OL1}$	$I_{SINK}=20mA$		0.1	0.4	V
	$V_{OL2}$	$I_{SINK}=100mA$		0.4	2.1	V
Output High Level	$V_{OH1}$	$I_{SOURCE}=20mA$	13	13.5		V
	$V_{OH2}$	$I_{SOURCE}=100mA$	12	13.2		V
Rise Time	$t_R$	$C_L=1nF$ , $T_J=25^\circ C$ (Note 2)		50	300	ns
Fall Time	$t_F$	$C_L=1nF$ , $T_J=25^\circ C$ (Note 2)		50	300	ns
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>						
Start-Up Threshold	$V_{START}$			7.7	8.0	V
Threshold Hysteresis	$V_H$			0.75		V
<b>TOTAL STANDBY CURRENT</b>						
Supply Current	$I_T$			17	21	mA

Notes: 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the specified terminal.

2. These parameters are not 100% tested in production, although guaranteed over the recommended operating conditions

3. Parameter measured at trip point of latch with  $V_{PIN5}=V_{REF}$ ,  $V_{PIN6}=0V$ .

4. Amplifier gain defined as:  $G = \frac{\Delta V_{PIN7}}{\Delta V_{PIN4}}$ ,  $V_{PIN4}=0\sim 1.0V$

5. Applies to UTC UC3846 only due to polarity of outputs.

6. Current into Pin 1 guaranteed to latch circuit in shutdown state.

7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

## ■ TEST CIRCUIT

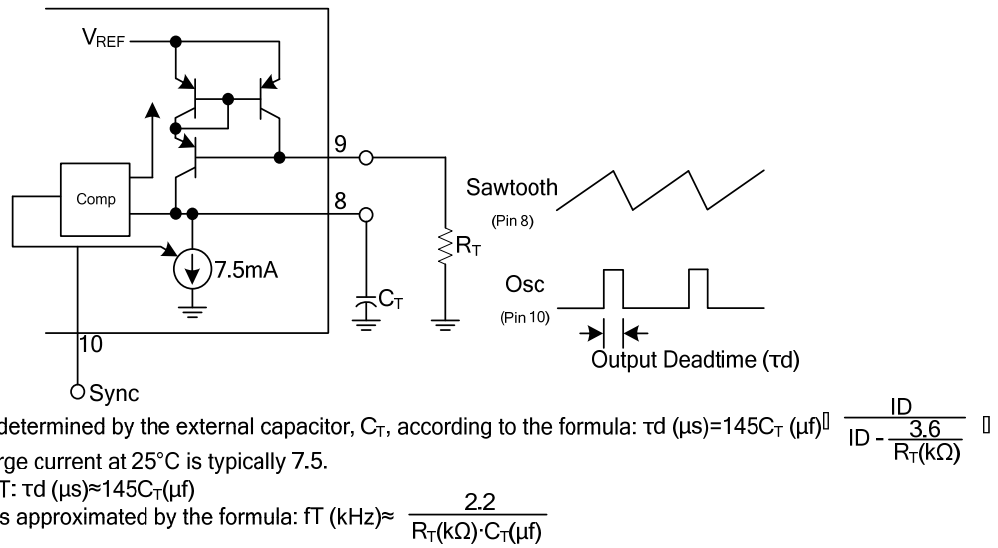


Figure 1. Oscillator Circuit

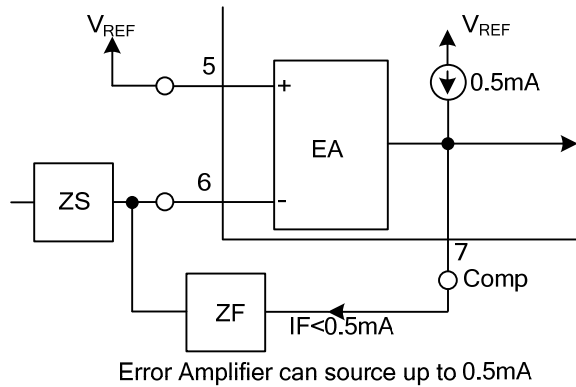


Figure 2. Error Amp Output Configuration

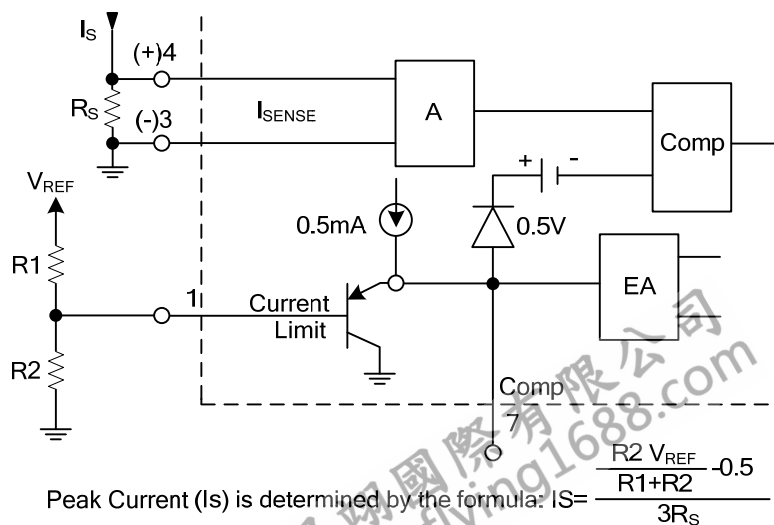


Figure 3. Pulse by Pulse Current Limiting

■ TEST CIRCUIT(Cont.)

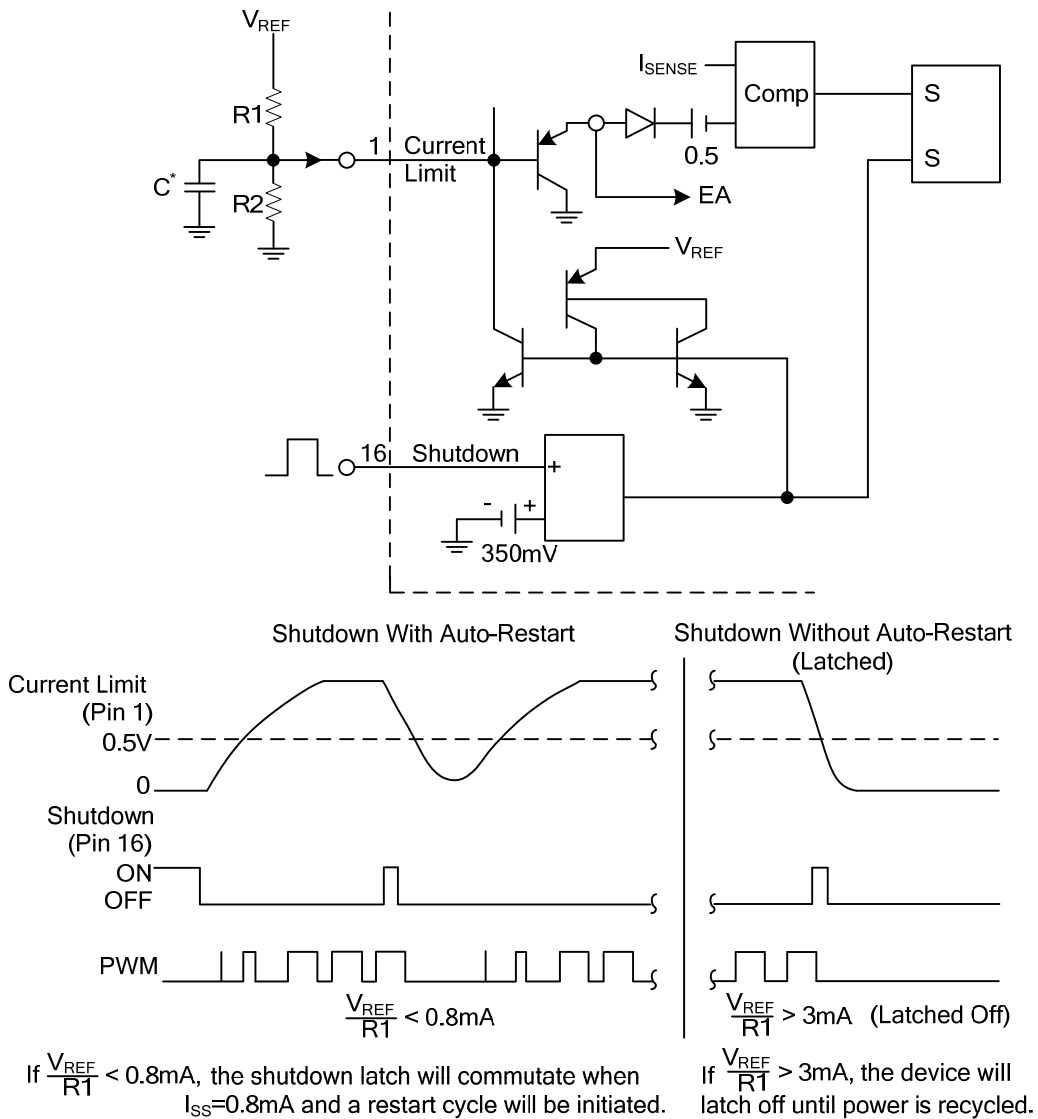
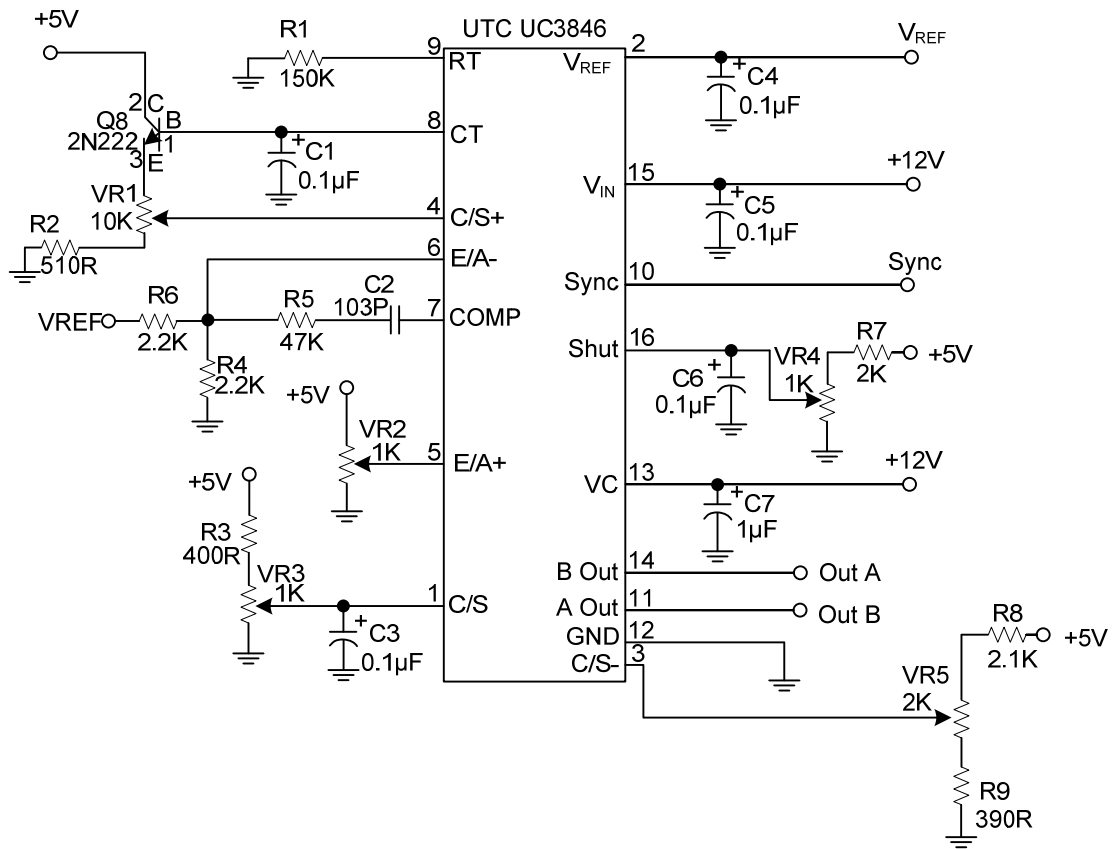


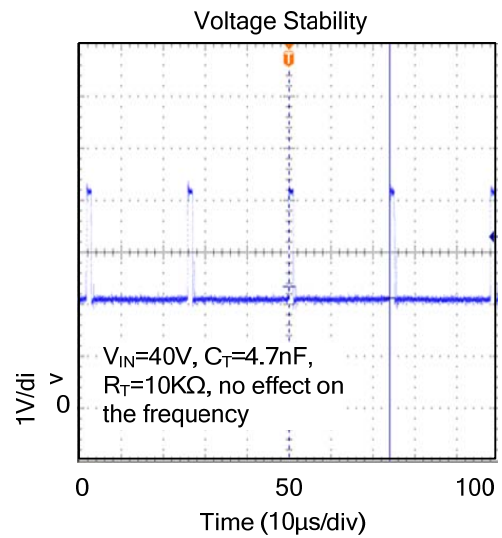
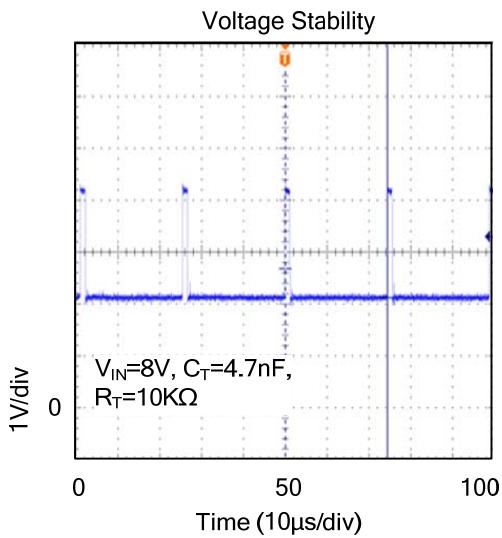
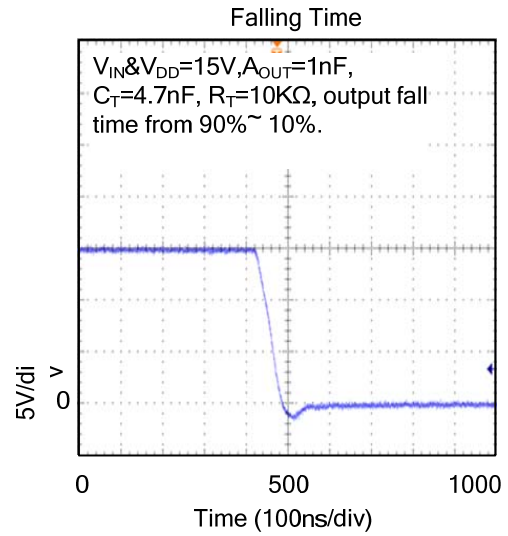
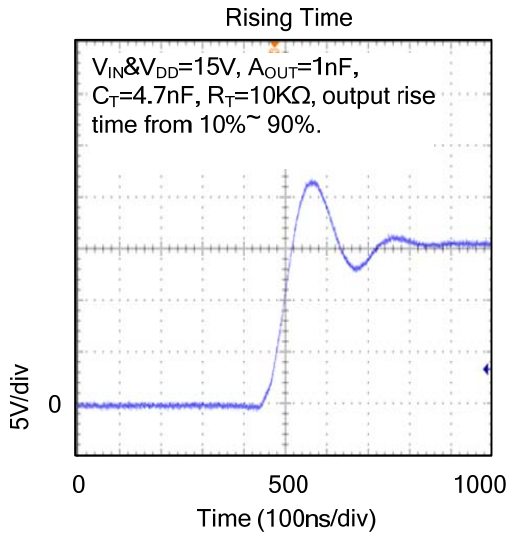
Figure 4. Soft Start and Shutdown /Restart Functions

### ■ TYPICAL APPLICATION CIRCUIT





■ TYPICAL CHARACTERISTICS



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