



UC4107

Preliminary

CMOS IC

TWO-STAGE HYSTERETIC LED DRIVER CONTROLLER

DESCRIPTION

The UTC **UC4107** is a two-stage controller with dual gate drivers consist of a Boost converter and a Buck converter. The advantage of the two-stage topology is highly compatible with Electronic Transformer in MR16/AR111 lighting market field applications.

The UTC **UC4107** is equipped with dual output gate drivers for external power MOSFETs, suitable for higher power applications.

FEATURES

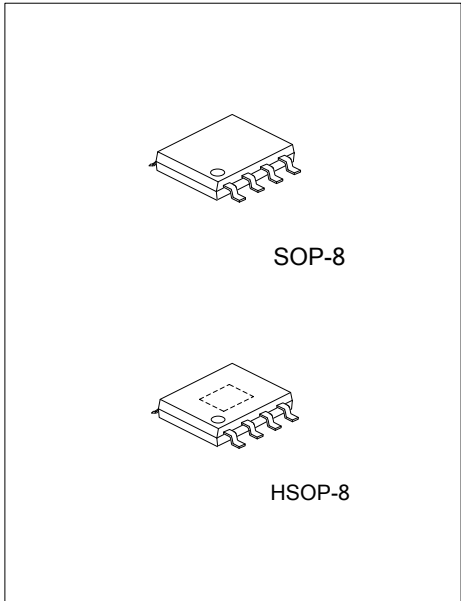
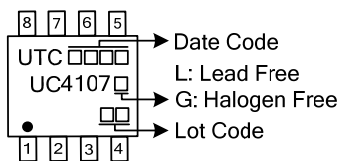
- * Topology: Boost+Buck
- * Input Voltage Range: 4.5V~40V
- * Adjustable Peak Input Current Control
- * Adjustable Boost Output Voltage
- * Independent Dual Stage Function
- * Adjustable LED Current
- * LED Current Accuracy: $\pm 5\%$
- * Input Under Voltage Lockout Detection
- * Thermal Shutdown Protection

ORDERING INFORMATION

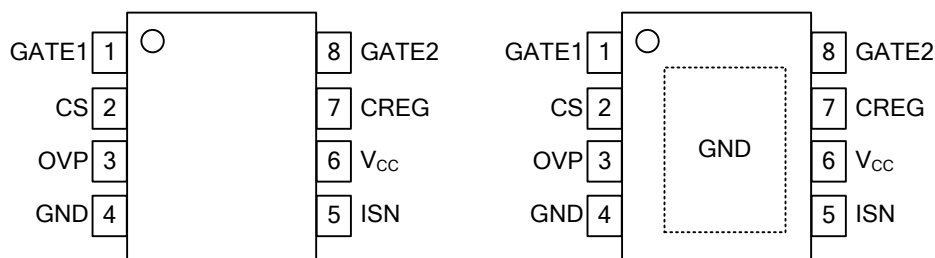
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC4107L-S08-R	UC4107G-S08-R	SOP-8	Tape Reel
UC4107L-SH2-R	UC4107G-SH2-R	HSOP-8	Tape Reel

<p>UC4107G-S08-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8, SH2: HSOP-8</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



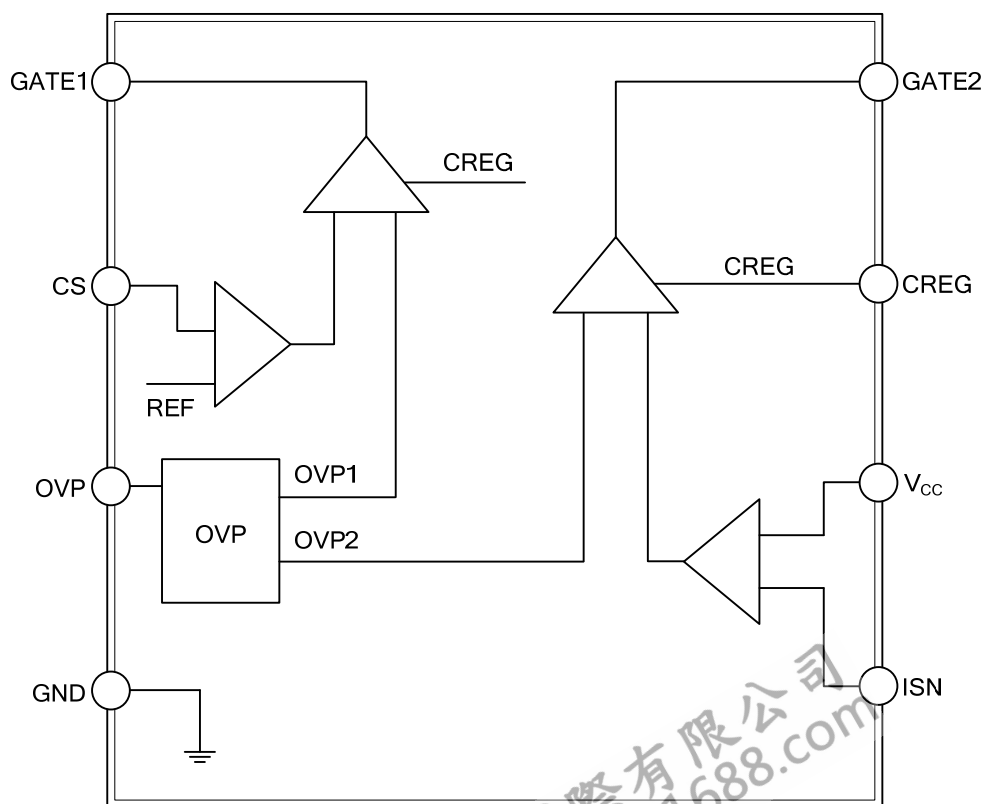
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GATE1	Gate Driver Output for External MOSFET Switch in the First Stage.
2	CS	Current Sense Input for External MOSFET Switch.
3	OVP	Over Voltage Protection Sense Input.
4	GND	Ground.
5	ISN	LED Current Sense Amplifier Negative Input.
6	V _{CC}	Supply Voltage Input. For good bypass, place a ceramic capacitor near the VCC pin.
7	CREG	Internal Regulator Output. Place an 1μF capacitor between the CREG and GND pins.
8	GATE2	Gate Driver Output for External MOSFET Switch in the Second Stage.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Input Voltage, V_{CC} to GND		-0.3 ~ 45	V
CS, GATE1, GATE2, CREG, OVP to GND		-0.3 ~ 6	V
V_{CC} To ISN	V_{ISN}	-1 ~ 3	V
Power Dissipation, @ $T_A=25^{\circ}\text{C}$	P_D	0.53	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Input Voltage	V_{CC}	4.5 ~ +40	V
Junction Temperature Range	T_J	-40 ~ +125	$^{\circ}\text{C}$
Ambient Temperature Range	T_A	-40 ~ +85	$^{\circ}\text{C}$

■ THERMAL DATA

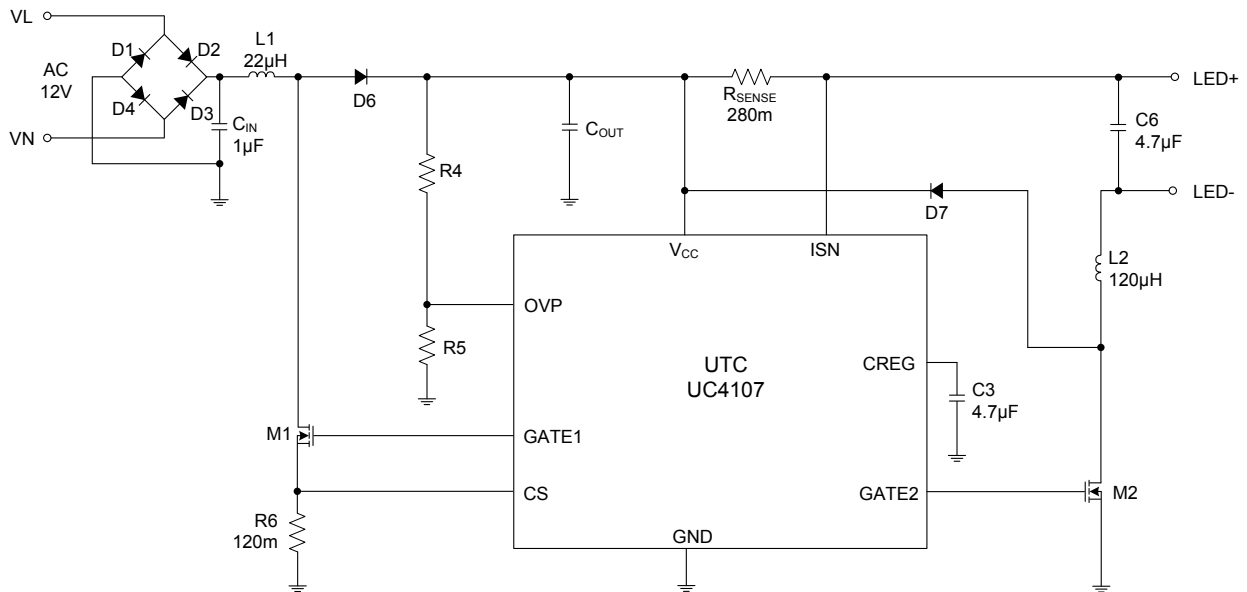
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	188	$^{\circ}\text{C/W}$

■ ELECTRICAL CHARACTERISTICS

($V_{CC}=10\text{V}$, No Load, $C_{LOAD}=1\text{nF}$, $T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CREG UVLO_ON	V_{UVOL_ON}	CS/OVP=0V	4	4.3	4.6	V
CREG UVLO_OFF	V_{UVOL_OFF}	CS/OVP=0V		4.2		V
V_{CC} Shutdown Current	I_{SHDN}	Before Start-Up, $V_{CC}=3.5\text{V}$		10		μA
V_{CC} Quiescent Current	I_Q	After Start-Up, $V_{CC}=5\text{V}$, GATE1 and GATE2 Stand Still		1.5		mA
Internal Reference Voltage	V_{CREG}			5		V
Internal Reference Voltage		$I_{CREG}=20\text{mA}$		4.9		V
CS Threshold Voltage	V_{CS}		215	240	265	mV
CS Pin Leakage Current	I_{CS}			1		μA
OVP High Level	V_{OVP_H}		1.71	1.9	2.09	V
OVP Low Level	V_{OVP_L}		1.44	1.6	1.76	V
OVP Pin Leakage Current	I_{OVP}			1		μA
GATE1 Duty Off-Time				1.5		μs
UGATE1 Drive Sink	$R_{UGATE1sk}$	Sink=50mA		2		Ω
LGATE1 Drive Source	$R_{LGATE1sr}$	Source=-50mA		1.25		Ω
GATE1 Default Pull Down Resistor				90		k Ω
ISN Threshold	V_{ISN}		123.5	130	136.5	mV
ISN Hysteresis	ΔV_{ISN}		10	15	20	%
ISN Pin Leakage Current	I_{ISN}			1		μA
UGATE2 Drive Sink	$R_{UGATE2sk}$	Sink=50mA		2		Ω
LGATE2 Drive Source	$R_{LGATE2sr}$	Source=-50mA		1.25		Ω
GATE2 Default Pull Down Resistor				90		k Ω
Thermal Shutdown Temperature	T_{SD}		140	155	170	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	ΔT_{SD}			35		$^{\circ}\text{C}$

■ TYPICAL APPLICATION CIRCUIT



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