



## UCD4023B

Preliminary

CMOS IC

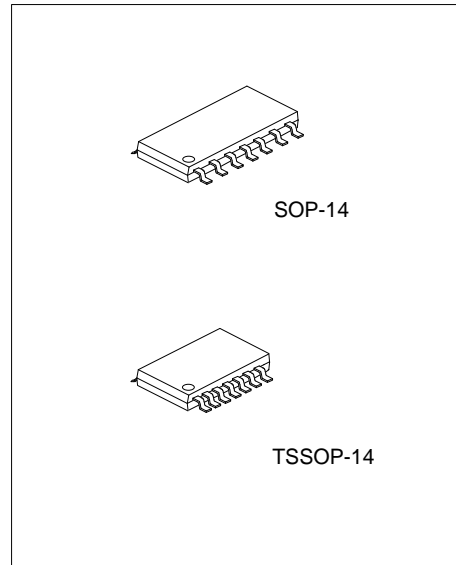
### TRIPLE 3-INPUT NAND GATE

#### DESCRIPTION

The **UCD4023B** contains three independent 3-input NAND gates, they perform the function  $Y = \overline{A \times B \times C}$  in positive logic.

#### FEATURES

- \* 5V-10V-15V Parametric Ratings
- \* Triple 3-Input NAND Gate
- \* Symmetrical Output Characteristics
- \* Maximum Input Current of 1uA at 15V Over Full Package Temperature Range

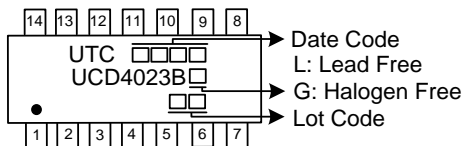


#### ORDERING INFORMATION

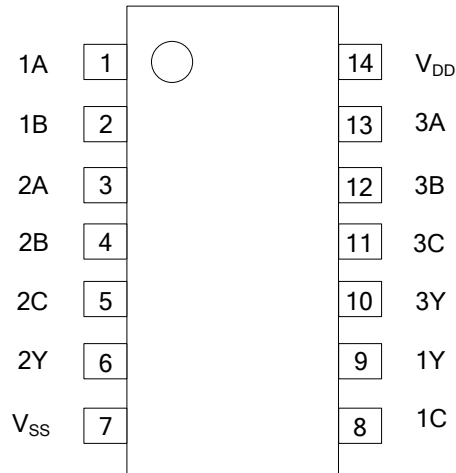
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4023BL-S14-R	UCD4023BG-S14-R	SOP-14	Tape Reel
UCD4023BL-P14-R	UCD4023BG-P14-R	TSSOP-14	Tape Reel

<p>UCD4023BG-S14-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) S14: SOP-14, P14: TSSOP-14</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



■ PIN CONFIGURATION

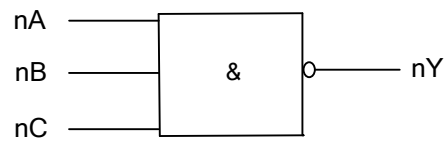
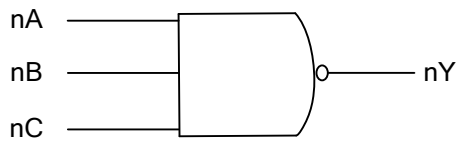


■ FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	INPUT(C)	OUTPUT(Y)
H	H	H	L
X	X	L	H
X	L	X	H
L	X	X	H

Note: X = DON'T CARE CASE

■ LOGIC DIAGRAM (positive logic)



■ **ABSOLUTE MAXIMUM RATING** ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	-0.5 ~ 18	V
Input Voltage	$V(nA, nB, nC)$	-0.5 ~ $V_{DD} + 0.5$	V
Output Voltage	$V(nY)$	-0.5 ~ $V_{DD} + 0.5$	V
Storage Temperature	$T_{STG}$	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{DD}$		3		15	V
Operating Temperature	$T_{OPR}$		-40		+85	$^\circ\text{C}$

■ **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	$V_{IH}$	$V_{DD}=5V, V_O=0.5V$	3.5	3		V
		$V_{DD}=10V, V_O=1.0V$	7.0	6		
		$V_{DD}=5V, V_O=1.5V$	11.0	9		
Low-Level Input Voltage	$V_{IL}$	$V_{DD}=5V, V_O=4.5V$		2	1.5	V
		$V_{DD}=10V, V_O=9.0V$		4	3.0	
		$V_{DD}=15V, V_O=13.5V$		6	4.0	
High-Level Output Voltage	$V_{OH}$	$V_{DD}=5V, \text{No Load}$	4.95	5		V
		$V_{DD}=10V, \text{No Load}$	9.95	10		
		$V_{DD}=15V, \text{No Load}$	14.95	15		
Low-Level Output Voltage	$V_{OL}$	$V_{DD}=5V, \text{No Load}$		0	0.05	V
		$V_{DD}=10V, \text{No Load}$		0	0.05	
		$V_{DD}=15V, \text{No Load}$		0	0.05	
High-Level Output Current (NOTE)	$I_{OH}$	$V_{DD}=5V, V_O=4.6V$	-0.44	-0.88		mA
		$V_{DD}=10V, V_O=9.5V$	-1.1	-2.25		
		$V_{DD}=15V, V_O=13.5V$	-3.0	-8.8		
Low-Level Output Current (NOTE)	$I_{OL}$	$V_{DD}=5V, V_O=0.4V$	0.44	0.88		mA
		$V_{DD}=10V, V_O=0.5V$	1.1	2.25		
		$V_{DD}=15V, V_O=1.5V$	3.0	8.8		
Input Leakage Current	$I_{I(LEAK)}$	$V_{DD}=15V, V_{IN}=V_{DD} \text{ or } GND$			$\pm 0.1$	$\mu\text{A}$
Quiescent Supply Current	$I_Q$	$V_{DD}=5V, V_{IN}=V_{DD} \text{ or } V_{SS}, I_{OUT}=0$		0.004	0.25	$\mu\text{A}$
		$V_{DD}=10V, V_{IN}=V_{DD} \text{ or } V_{SS}, I_{OUT}=0$		0.005	0.5	
		$V_{DD}=15V, V_{IN}=V_{DD} \text{ or } V_{SS}, I_{OUT}=0$		0.006	1.0	

Note:  $I_{OL}$  and  $I_{OH}$  are tested one output at a time

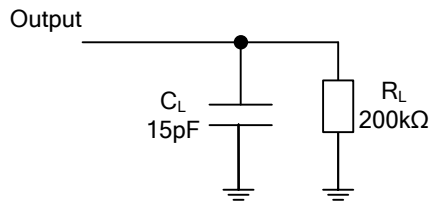
■ **SWITCHING CHARACTERISTICS** ( $T_A=25^\circ\text{C}$ , Input:  $t_R=t_F=20\text{ns}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	$t_{PLH}$	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		75	100	ns
		$V_{DD}=10\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		40	50	
	$t_{PHL}$	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		75	100	ns
		$V_{DD}=10\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		40	50	
Transition Time Low-to-High Level	$t_{TLH}$	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		75	125	ns
		$V_{DD}=10\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		40	75	
Transition Time High-to-Low Level	$t_{THL}$	$V_{DD}=5\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		75	150	ns
		$V_{DD}=10\text{V}$ , $C_L=15\text{pF}$ , $R_L=200\text{k}\Omega$		50	100	

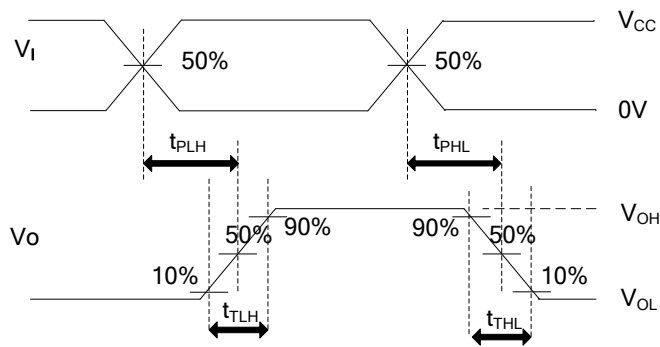
■ **OPERATING CHARACTERISTICS** ( $T_A=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	$C_{IN}$	Any Input		5	7.5	pF
Power Dissipation Capacitance	$C_{PD}$	Any Gate		17		pF

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit



Propagation Delay Times

Note:  $C_L$  includes probe and jig capacitance.

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