

## UD4840-H

## **Power MOSFET**

# 6A, 40V DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

## DESCRIPTION

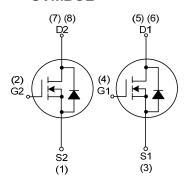
The UTC **UD4840-H** is a dual N-Channel enhancement mode field effect transistor, it uses UTC's advanced technology to provide customers with a minimum on-state resistance and low gate charge, etc.

The UTC **UD4840-H** is suitable for use as a load switch or in PWM applications.

## FEATURES

- \* R<sub>DS(ON)</sub>< 32 mΩ @ V<sub>GS</sub>=10V, I<sub>D</sub>=6A
- $R_{DS(ON)}$  < 42 m $\Omega$  @ V<sub>GS</sub>=4.5V, I<sub>D</sub>=5A
- \* Low gate charge

#### ■ SYMBOL

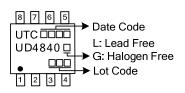


#### ORDERING INFORMATION

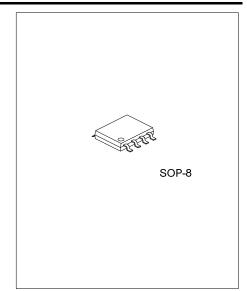
Ordering Number		Dookogo		Pin Assignment							Decking		
Lead Free	Halogen Free	Package		1	2	3	4	5	6	7	8	Packing	
UD4840L-S08-R	UD4840G-S08-R	SOP-8		S2	G2	S1	G1	D1	D1	D2	D2	Tape Reel	
Note: Pin Assignment: G: Gate D: Drain S: Source													
UD4840G-S08-R			(1) R:	Тар	e Re	el							
(2)Package Type			(2) SC	)8: S	OP-8	8							

(3) G: Halogen Free and Lead Free, L: Lead Free

## ■ MARKING



- (3)Green Package



## ■ **ABSOLUTE MAXIMUM RATINGS** (T<sub>A</sub>=25°C, unless otherwise noted)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V <sub>DSS</sub>	40	V
Gate-Source Voltage		V <sub>GSS</sub>	±20	V
Continuous Drain Current	T <sub>A</sub> =25°C		6	А
(Note 1)	T <sub>A</sub> =70°C	I <sub>D</sub>	5	А
Pulsed Drain Current (Note 2)		I <sub>DM</sub>	20	А
Single Pulsed Avalanche Energy	Single Pulsed (Note 3)	E <sub>AS</sub>	5	mJ
Dower Dissinction	T <sub>A</sub> =25°C	P	2	W
Power Dissipation	T <sub>A</sub> =70°C	PD	1.28	W
Junction Temperature		TJ	-55 ~ +150	°C
Storage Temperature Range		T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L = 0.1mH,  $I_{AS}$  = 10A,  $V_{DD}$  = 20V,  $R_G$  = 25 $\Omega$ , Starting  $T_J$  = 25°C.

## THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	
lunction to Ambient (Note 1)	t≤10s	0		48	62.5	°C/W	
Junction to Ambient (Note 1)	Steady-State	θ <sub>JA</sub>		74	110	°C/W	
Junction to Lead (Note 3)	Steady-State	θ <sub>JC</sub>		35	50	°C/W	

Notes: 1. The value of θ<sub>JA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤10s thermal resistance rating.

2. Repetitive rating, pulse width limited by junction temperature.

3. The  $\theta_{JA}$  is the sum of the thermal impedence from junction to lead  $\theta_{JL}$  and lead to ambient.



## ■ ELECTRICAL CHARACTERISTICS (TJ=25°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	40			V
Zara Cata Valtaga Drain Current		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V			1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C			5	μA
Cate Source Leakage Current	d ,	V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V			+100	nA
Gate-Source Leakage Current Reverse	e I <sub>GSS</sub>	V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	1.5	2.3	3	V
On State Drain Current	I <sub>D(ON)</sub>	$V_{DS}$ =5V, $V_{GS}$ =10V	20			А
		V <sub>GS</sub> =10V, I <sub>D</sub> =6A			32	mΩ
Static Drain-Source On-State Resistance	e R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =6A, T <sub>J</sub> =125°C			48	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A			42	mΩ
Forward Transconductance	<b>g</b> <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =6A		22		S
DYNAMIC PARAMETERS						
Input Capacitance	C <sub>ISS</sub>			400		pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		50		рF
Reverse Transfer Capacitance	C <sub>RSS</sub>			25		pF
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		2.7		Ω
SWITCHING PARAMETERS		_				
Total Gate Charge	Q <sub>G</sub>	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =32V, I <sub>D</sub> =6.0A I <sub>G</sub> =1mA		7.2		nC
	<b>~</b> 0			30		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =1.0A		1.0		nC
Gate to Drain Charge		—I <sub>G</sub> =100μA		2.0		nC
Turn-ON Delay Time	t <sub>D(ON)</sub>	1		115		ns
Rise Time				190		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>	$R_{G}=25\Omega$		5		ns
Fall-Time		1 -		19		ns
SOURCE- DRAIN DIODE RATINGS AN		RISTICS	1		1	1
Maximum Body-Diode Continuous Curre	-			1	3	Α
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.77	1	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			20.5		ns
Body Diode Reverse Recovery Charge	Qrr	—I <sub>F</sub> =6A, dI/dt=100A/μs		14.5		nC



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