



## UD4N03-H

Preliminary

Power MOSFET

### 4A, 30V DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

#### DESCRIPTION

The UTC **UD4N03-H** is a dual N-Channel enhancement mode field effect transistor, it uses UTC's advanced technology to provide customers with a minimum on-state resistance and low gate charge, etc.

The UTC **UD4N03-H** is suitable for use as a load switch or in PWM applications.

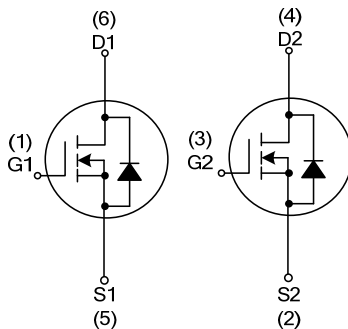
#### FEATURES

\*  $R_{DS(ON)} < 38\text{ m}\Omega$  @  $V_{GS}=10\text{V}$ ,  $I_D=3.5\text{A}$

$R_{DS(ON)} < 72\text{ m}\Omega$  @  $V_{GS}=4.5\text{V}$ ,  $I_D=2.5\text{A}$

\* Low gate charge

#### SYMBOL



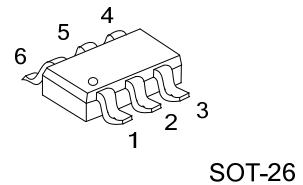
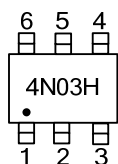
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing
Lead Free	Halogen Free		1	2	3	4	5	6	
UD4N03L-AG6-R	UD4N03G-AG6-R	SOT-26	G1	S2	G2	D2	S1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<b>UD4N03G-AG6-R</b>		(1)Packing Type	(1) R: Tape Reel
		(2)Package Type	(2) AG6: SOT-26
		(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

#### MARKING



SOT-26

■ ABSOLUTE MAXIMUM RATINGS ( $T_A=25^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	4	A
Pulsed Drain Current (Note 2)	$I_{DM}$	16	A
Peak Diode Recovery $dv/dt$ (Note 4)	$dv/dt$	1.7	V/ns
Power Dissipation	$P_D$	1.14	W
Junction Temperature	$T_J$	$-55 \sim +150$	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	$-55 \sim +150$	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $I_{SD} \leq 4.0\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J = 25^{\circ}\text{C}$ .

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	150	$^{\circ}\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	80	$^{\circ}\text{C}/\text{W}$

Note: Repetitive Rating: Pulse width limited by maximum junction temperature.

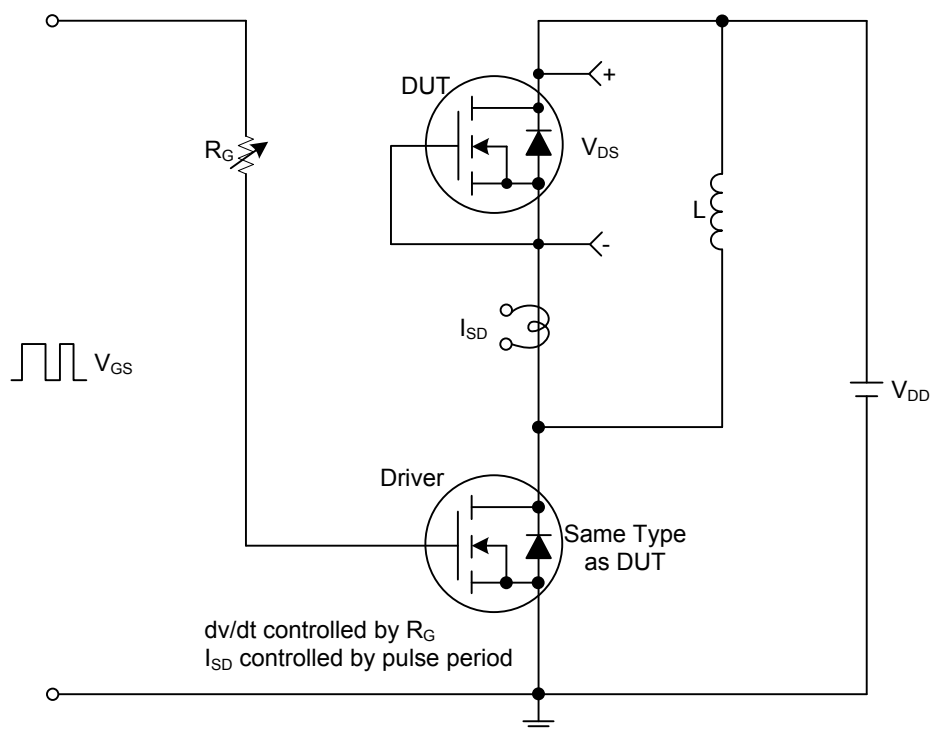
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
Zero Gate Voltage Drain Current		I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			1	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub>	V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V			+100	nA
	Reverse		V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A			38	mΩ
			V <sub>GS</sub> =4.5V, I <sub>D</sub> =2.5A			72	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		200		pF
Output Capacitance		C <sub>OSS</sub>			37		pF
Reverse Transfer Capacitance		C <sub>RSS</sub>			32		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q <sub>G</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =1.0A I <sub>G</sub> =100μA		13		nC
Gate to Source Charge		Q <sub>GS</sub>			0.8		nC
Gate to Drain Charge		Q <sub>GD</sub>			1.4		nC
Turn-ON Delay Time		t <sub>D(ON)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, , I <sub>D</sub> =1.0A R <sub>G</sub> =25Ω		22		ns
Rise Time		t <sub>R</sub>			30		ns
Turn-OFF Delay Time		t <sub>D(OFF)</sub>			98		ns
Fall-Time		t <sub>F</sub>			70		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I <sub>S</sub>				4	A
Maximum Body-Diode Pulsed Current		I <sub>SM</sub>				16	A
Diode Forward Voltage		V <sub>SD</sub>	I <sub>S</sub> =3.5A, V <sub>GS</sub> =0V			1.2	V
Body Diode Reverse Recovery Time		t <sub>rr</sub>	I <sub>F</sub> =4.0A, dI/dt=100A/μs		780		ns
Body Diode Reverse Recovery Charge		Q <sub>rr</sub>			2.23		μC

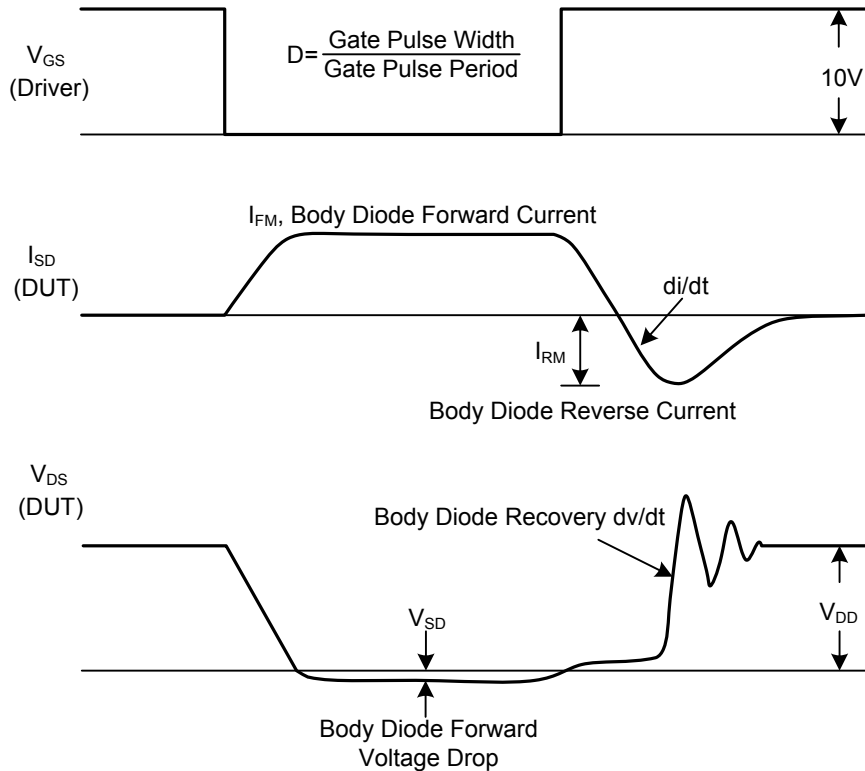
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

2. Essentially independent of operating temperature

# ■ TEST CIRCUITS AND WAVEFORMS



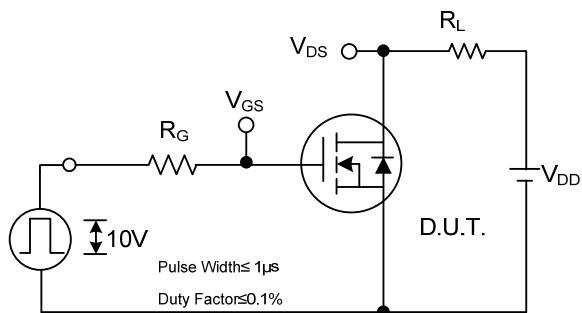
**Peak Diode Recovery dv/dt Test Circuit**



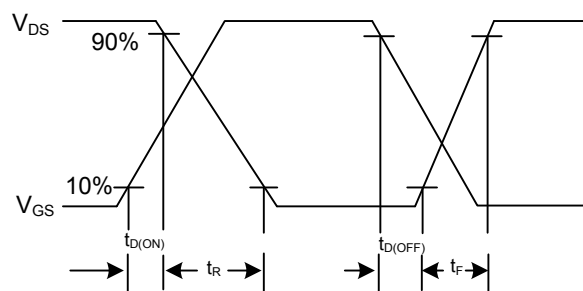
**Peak Diode Recovery dv/dt Test Circuit and Waveforms**

**Peak Diode Recovery dv/dt Waveforms**

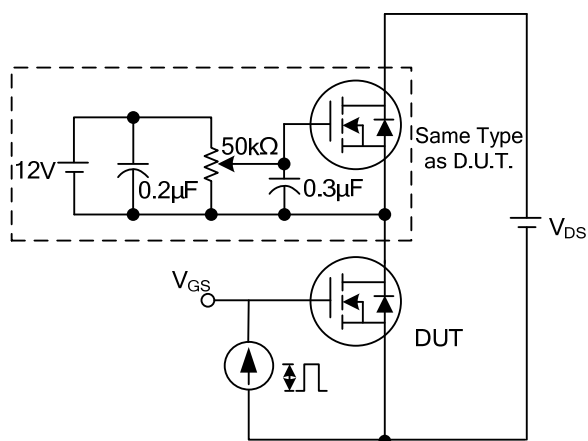
## ■ TEST CIRCUITS AND WAVEFORMS



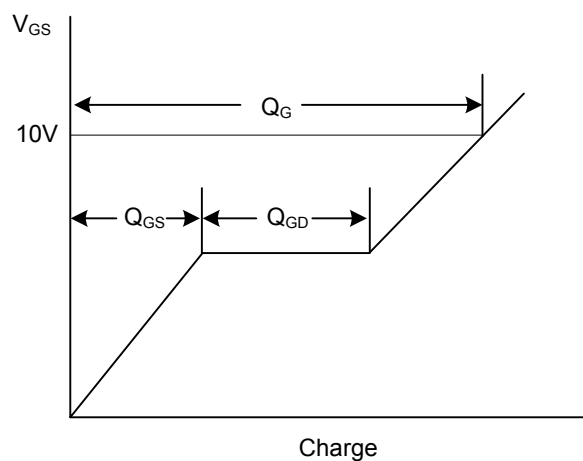
Switching Test Circuit



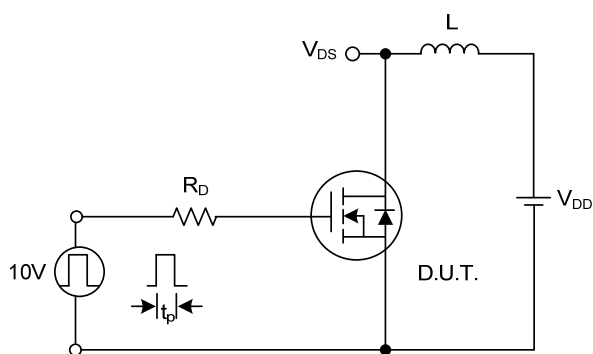
Switching Waveforms



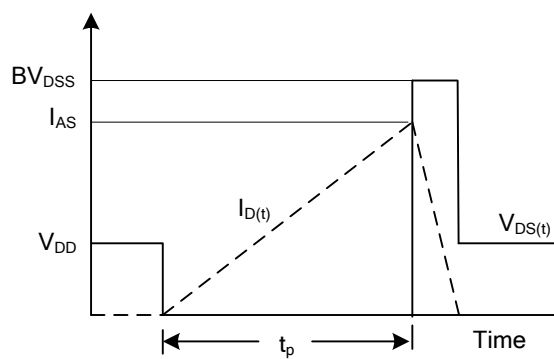
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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