

UNISONIC TECHNOLOGIES CO., LTD

UF3N20 Preliminary Power MOSFET

SOP-8

QW-R205-106.a

3A, 200V N-CHANNEL POWER MOSFET

■ DESCRIPTION

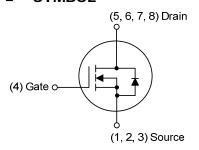
The UTC **UF3N20** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **UF3N20** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

■ FEATURES

- * $R_{DS(ON)}$ < 200m Ω @ V_{GS} =10V, I_D =1.5A
- * High switching speed
- * 100% avalanche tested

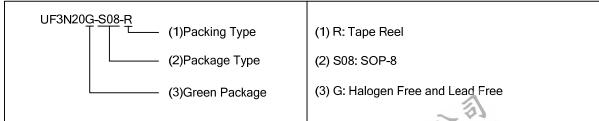
■ SYMBOL



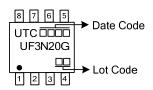
ORDERING INFORMATION

| | Ordering Number | Dookogo | Pin Assignment | | | | | | | | Dooking | |
|--|-----------------|---------|----------------|---|---|---|---|---|---|---|-----------|--|
| | | Package | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Packing | |
| | UF3N20G-S08-R | SOP-8 | S | S | S | G | D | D | D | D | Tape Reel | |

Note: Pin Assignment: S: Source G: Gate D: Drain



■ MARKING



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ABSOLUTE MAXIMUM RATINGS

| PARAMET | ER | SYMBOL | RATINGS | UNIT |
|---------------------------|------------|--------------------|----------|------|
| Drain-Source Voltage | | V_{DSS} | 200 | V |
| Gate-Source Voltage | | V_{GSS} | ±20 | V |
| Continuous Drain Current | Continuous | I _D | 3 | Α |
| Continuous Drain Current | Pulsed | I _{DM} 12 | | |
| Avalanche Energy | | E _{AS} | 52 | mJ |
| Power Dissipation | | P_{D} | 4.5 | mW |
| Junction Temperature | | T_J | +150 | °C |
| Storage Temperature Range | 9 | T _{STG} | -55~+150 | °C |

Preliminary

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

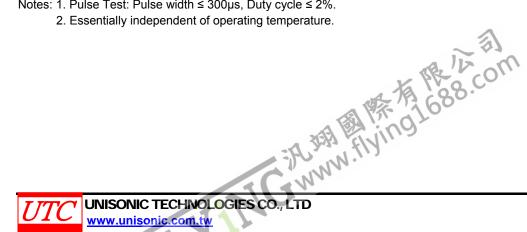
- 2. Repetitive Rating: Pulse width limited by T_J.
- 3. L=55mH, I_{AS} =2.0A, V_{DD} =50V, R_{G} =25 Ω , Starting T_{J} = 25°C
- 4. $I_{SD} \le 2.4$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25$ °C

ELECTRICAL CHARACTERISTICS

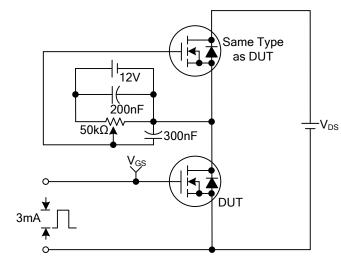
| PARAMETER | | SYMBOL | TEST CONDITIONS | TYP | MAX | UNIT | |
|----------------------------------|-------------------|---------------------|--|-----|------|------|----|
| OFF CHARACTERISTICS | | | | | | | |
| Drain-Source Breakdown Voltag | je | BV_{DSS} | $I_D=250\mu A,\ V_{GS}=0V$ | 200 | | | V |
| Drain-Source Leakage Current | | I _{DSS} | V _{DS} =200V | | | 1 | μA |
| Coto Source Leakage Current Forw | | 1 | V_{GS} =+20V, V_{DS} =0V | | | 10 | μΑ |
| Gate-Source Leakage Current | Reverse | I _{GSS} | V _{GS} =-20V, V _{DS} =0V | | | -10 | μΑ |
| ON CHARACTERISTICS | | | | | | | |
| Gate Threshold Voltage | | $V_{GS(TH)}$ | I _D =250μA | 1.0 | | 3.0 | V |
| Static Drain-Source On-State Re | esistance | R _{DS(ON)} | V_{GS} =10V, I_D =1.5A | | | 200 | mΩ |
| DYNAMIC PARAMETERS | | | | | | | |
| Input Capacitance | | C _{ISS} | | | 1530 | | pF |
| Output Capacitance | | Coss | V_{GS} =0V, V_{DS} =25V, f=1MHz | | 145 | | pF |
| Reverse Transfer Capacitance | | C_{RSS} | | | 8 | | pF |
| SWITCHING PARAMETERS | | | | | | | |
| Total Gate Charge | | Q_G | V _{GS} =10V, V _{DS} =50V, I _D =1.3A | | 160 | | nC |
| Gate to Source Charge | | Q_GS | -I _G =100μA (Note 1, 2) | | 6.0 | | nC |
| Gate to Drain Charge | e to Drain Charge | | IG-100μΑ (Note 1, 2) | | 3.2 | | nC |
| urn-ON Delay Time | | $t_{D(ON)}$ | | | 36 | | ns |
| Rise Time | | t_R | V_{GS} =10V, V_{DD} =30V, R_{G} =25 Ω , | | 28 | | ns |
| Turn-OFF Delay Time | | t _{D(OFF)} | I _D =0.5A (Note 1, 2) | | 490 | | ns |
| Fall-Time | | t_{F} | | | 64 | | ns |
| SOURCE- DRAIN DIODE RATI | NGS AND (| CHARACTERI | STICS | | | | |
| Maximum Body-Diode Continuo | us Current | Is | | | | 3 | Α |
| Maximum Body-Diode Pulsed C | urrent | I _{SM} | | | | 12 | Α |
| Drain-Source Diode Forward Vo | ltage | V_{SD} | I _S =3A | | | 1.3 | V |
| | | | | | | | |

Notes: 1. Pulse Test: Pulse width ≤ 300µs, Duty cycle ≤ 2%.

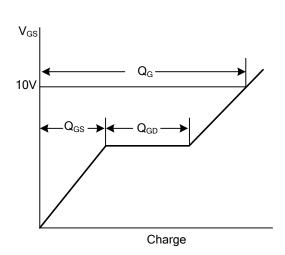
2. Essentially independent of operating temperature.



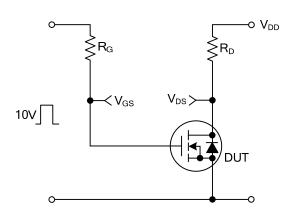
TEST CIRCUITS AND WAVEFORMS



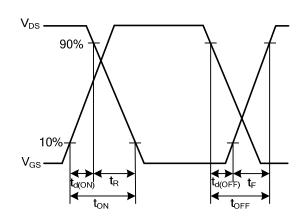
Gate Charge Test Circuit



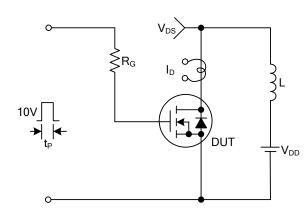
Gate Charge Waveforms



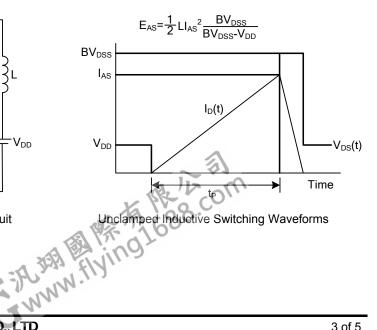
Resistive Switching Test Circuit



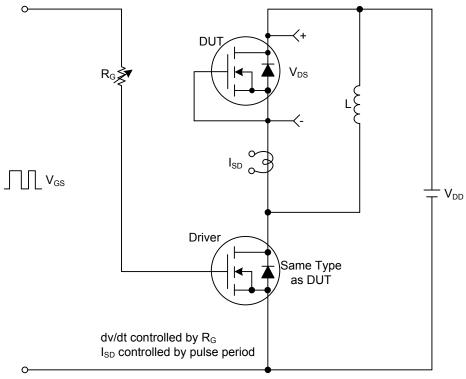
Resistive Switching Waveforms



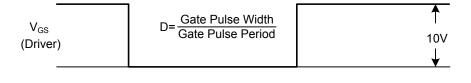
Unclamped Inductive Switching Test Circuit

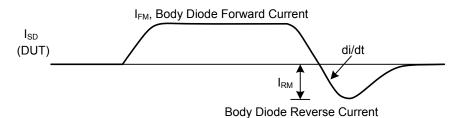


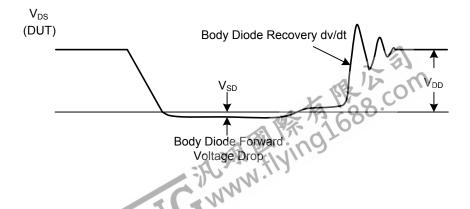
■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms







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