



UF40N08

Preliminary

Power MOSFET

**40A, 80V N-CHANNEL
POWER MOSFET**

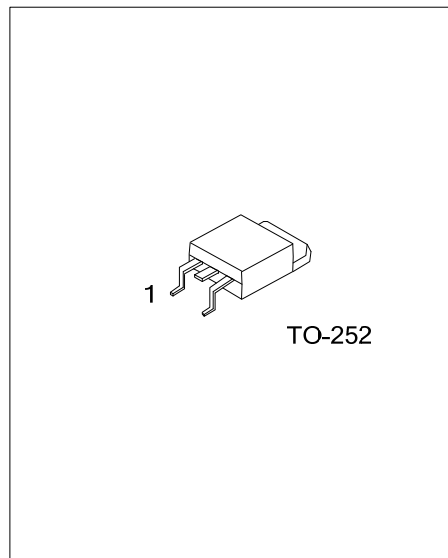
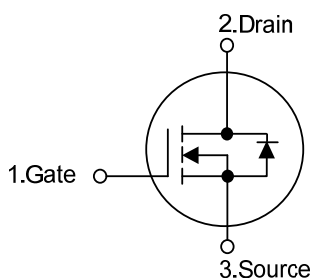
■ DESCRIPTION

The UTC **UF40N08** is a high voltage power MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

■ FEATURES

- * $R_{DS(ON)} < 28\text{ m}\Omega @ V_{GS}=10V, I_D=20A$
- * High switching speed
- * 100% avalanche tested

■ SYMBOL



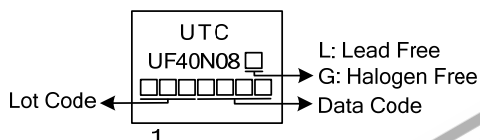
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF40N08L-TN3-R	UF40N08G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UF40N08G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	80	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	40
	Pulsed	I_{DM}	160
Avalanche Current (Note 2)	I_{AR}	22.5	A
Avalanche Energy	E_{AS}	202	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	13	V/ns
Power Dissipation	P_D	1.1	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.8\text{ mH}$, $I_{AS}=22.5\text{ A}$, $V_{DD}=50\text{ V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	1.92	$^\circ\text{C}/\text{W}$

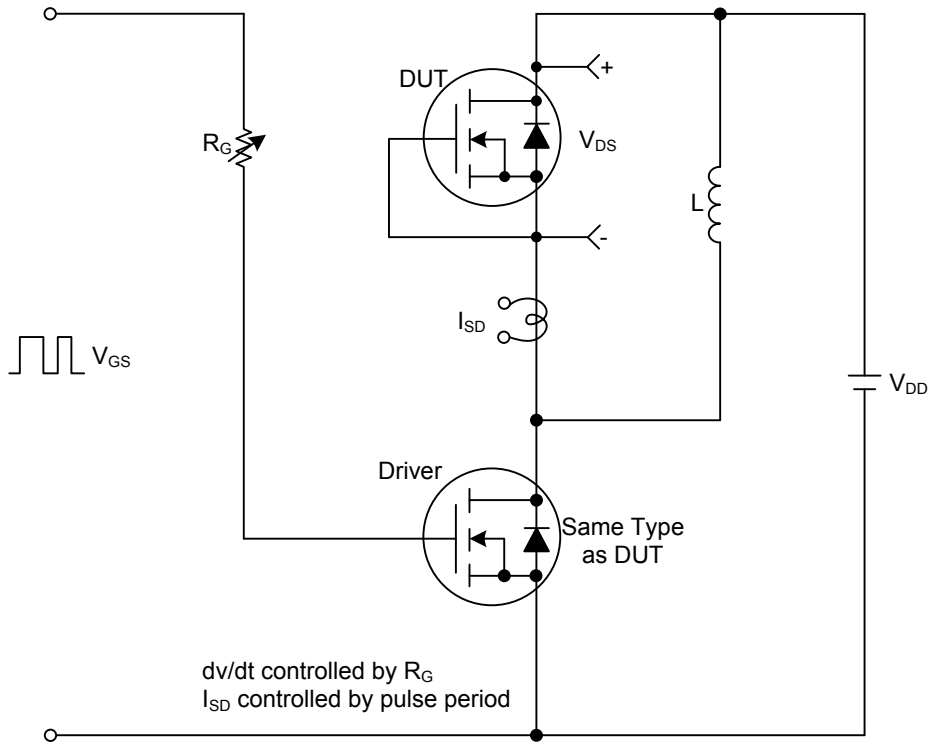
■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\ \mu\text{A}$, $V_{GS}=0\text{V}$	80			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	Forward	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			10	μA
	Reverse	$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-10	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D=250\ \mu\text{A}$, $V_{DS}=V_{GS}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=20\text{A}$			28	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1\text{MHz}$		1480		pF
Output Capacitance	C_{OSS}			286		pF
Reverse Transfer Capacitance	C_{RSS}			35		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $I_D=1.3\text{A}$ $I_G=100\ \mu\text{A}$ (Note 1, 2)		123		nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain Charge	Q_{GD}			13		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{GS}=10\text{V}$, $V_{DD}=30\text{V}$, $R_G=25\ \Omega$, $I_D=0.5\text{A}$ (Note 1, 2)		68		ns
Rise Time	t_R			64		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			400		ns
Fall-Time	t_F			100		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				40	A
Maximum Body-Diode Pulsed Current	I_{SM}				160	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=20\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=40\text{A}$, $V_{GS}=0\text{V}$		62		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{A}/\mu\text{s}$		0.15		μC

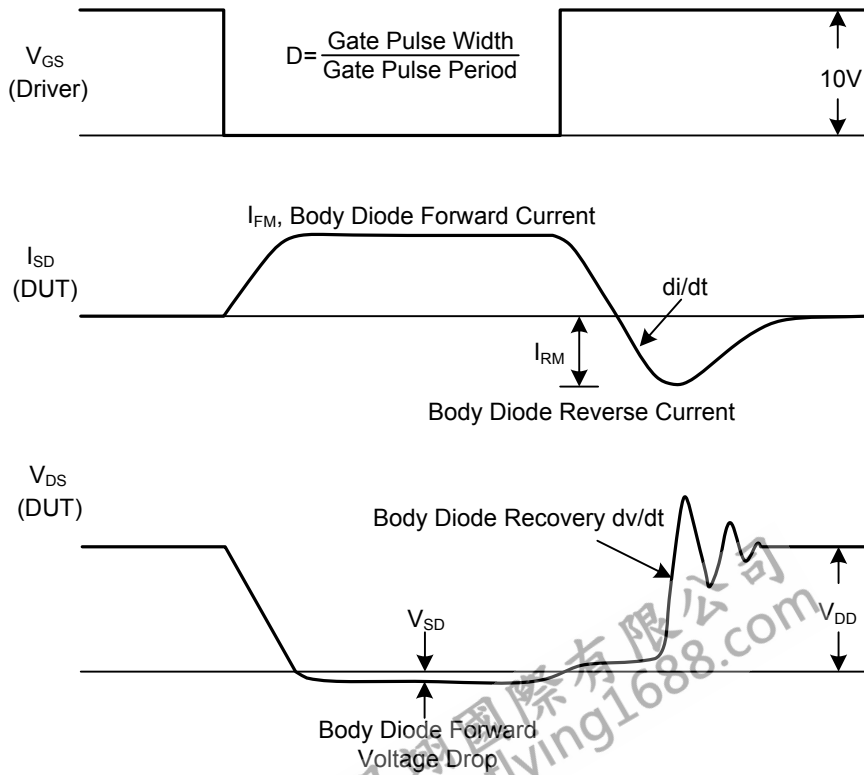
Notes: 1. Pulse Test: Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

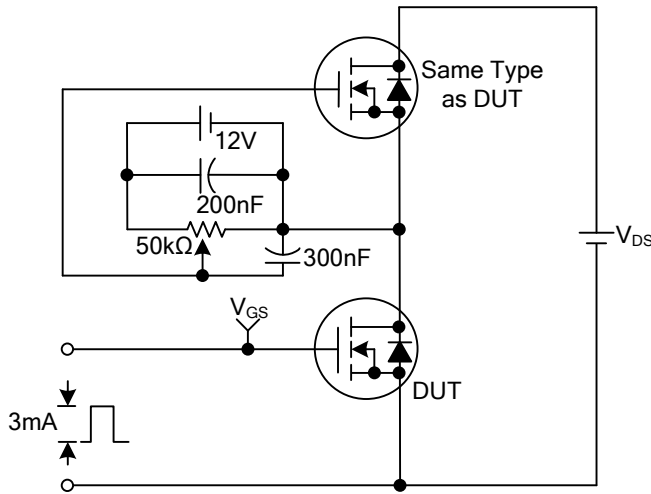


Peak Diode Recovery dv/dt Test Circuit

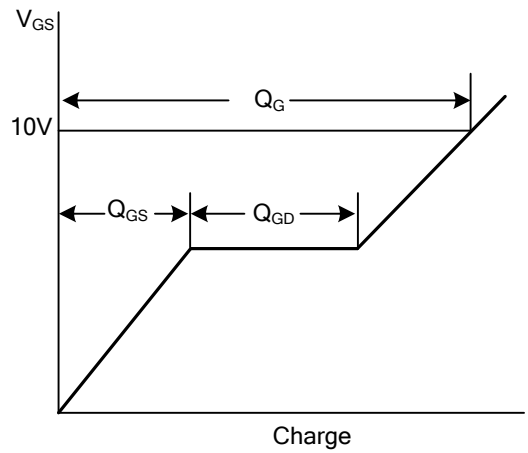


Peak Diode Recovery dv/dt Waveforms

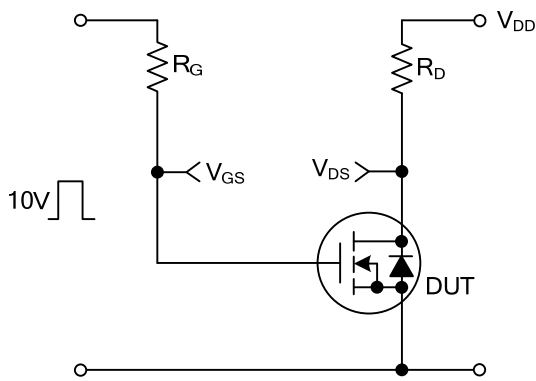
■ TEST CIRCUITS AND WAVEFORMS



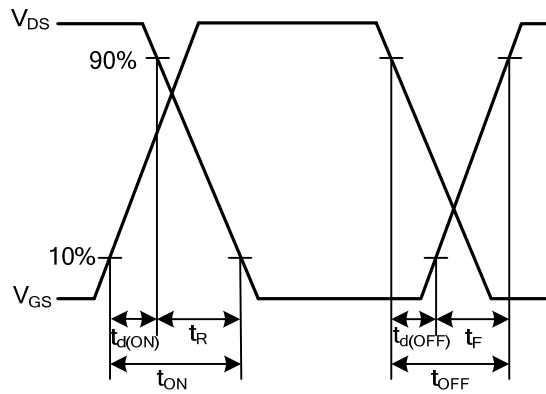
Gate Charge Test Circuit



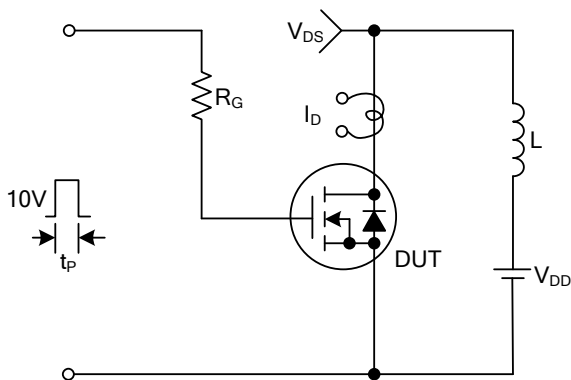
Gate Charge Waveforms



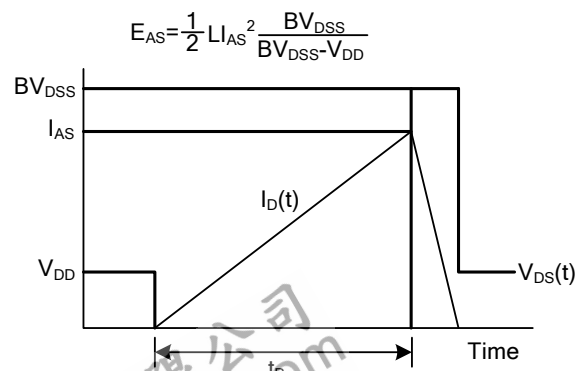
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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