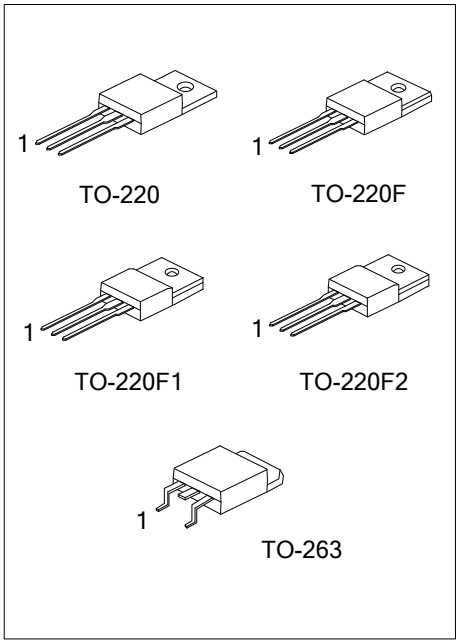
# UF740

**Power MOSFET**

## 10A, 400V, 0.55Ω N-CHANNEL POWER MOSFET



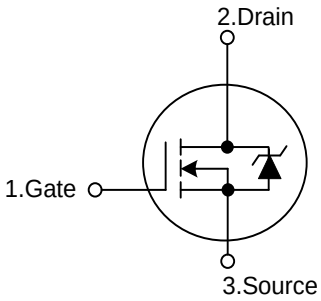

### ■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

### ■ FEATURES

* 10A, 400V, $R_{DS(ON)}$(0.55Ω)
* Single Pulse Avalanche Energy Rated
* Rugged - SOA is Power Dissipation Limited
* Fast Switching Speeds
* Linear Transfer Characteristics
* High Input Impedance

### ■ SYMBOL




### ■ ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | Packing |
|---|---|---|---|---|---|---|
| Lead Free | Halogen Free | | 1 | 2 | 3 | |
| UF740L-TA3-T | UF740G-TA3-T | TO-220 | G | D | S | Tube |
| UF740L-TF1-T | UF740G-TF1-T | TO-220F1 | G | D | S | Tube |
| UF740L-TF2-T | UF740G-TF2-T | TO-220F2 | G | D | S | Tube |
| UF740L-TF3-T | UF740G-TF3-T | TO-220F | G | D | S | Tube |
| UF740L-TQ2-T | UF740G-TQ2-T | TO-263 | G | D | S | Tube |
| UF740L-TQ2-R | UF740G-TQ2-R | TO-263 | G | D | S | Tape Reel |

Note: Pin Assignment: G: Gate D: Drain S: Source

UF740L-TA3-T
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) R: Tape Reel, T: Tube
(2) TA3: TO-220, TF1: TO-220F1, TF2: TO-220F2, TF3: TO-220F, TQ2: TO-263
(3) L: Lead Free, G: Halogen Free

## ■ ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25°C, Unless Otherwise Specified)

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Drain to Source Voltage ($T_J$ =25°C~125°C) | | $V_{DS}$ | 400 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) ($T_J$ =25°C~125°C) | | $V_{DGR}$ | 400 | V |
| Gate to Source Voltage | | $V_{GS}$ | ±20 | V |
| Drain Current | Continuous | $I_D$ | 10 | A |
| | $T_C$ = 100°C | $I_D$ | 6.3 | A |
| | Pulsed | $I_{DM}$ | 40 | A |
| Avalanche Energy | Single Pulsed (Note 3) | $E_{AS}$ | 520 | mJ |
| Power Dissipation | TO-220/TO-263 | $P_D$ | 125 | W |
| | TO-220F/TO-220F1 | | 44 | |
| | TO-220F2 | | 46 | |
| Derating above 25°C | TO-220/TO-263 | | 1.0 | W/°C |
| | TO-220F/TO-220F1 | | 0.35 | |
| | TO-220F2 | | 0.37 | |
| Junction Temperature | | $T_J$ | +150 | °C |
| Operating Temperature | | $T_{OPR}$ | -55 ~ +150 | °C |
| Storage Temperature | | $T_{STG}$ | -55 ~ +150 | °C |

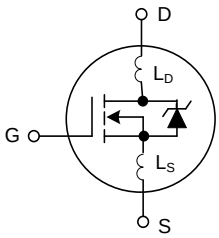
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

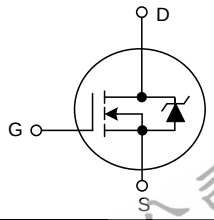
## ■ THERMAL DATA

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Junction to Ambient | | $\theta_{JA}$ | 62.5 | °C/W |
| Junction to Case | TO-220/TO-263 | $\theta_{Jc}$ | 1.0 | °C/W |
| | TO-220F/TO-220F1 | | 2.86 | |
| | TO-220F2 | | 2.72 | |

## ■ ELECTRICAL CHARACTERISTICS ($T_C$ =25°C, Unless Otherwise Specified.)

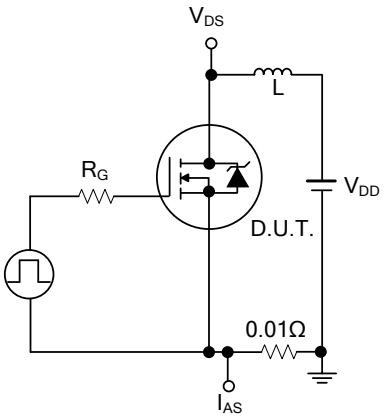
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 400 | | | V |
| Gate to Threshold Voltage | $V_{GS(THR)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 2.0 | | 4.0 | V |
| On-State Drain Current (Note 1) | $I_{D(ON)}$ | $V_{DS}$ >$I_{D(ON)}$ x $R_{DS(ON)MAX}$, $V_{GS}$ =10V | 10 | | | A |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = Rated $BV_{DSS}$, $V_{GS}$ = 0V | | | 25 | μA |
| | | $V_{DS}$=0.8 x Rated $BV_{DSS}$, $V_{GS}$=0V,$T_J$=125°C | | | 250 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20V | | | ±500 | nA |
| Drain to Source On Resistance | $R_{DS(ON)}$ | $V_{GS}$ = 10V, $I_D$ = 5.2A (Note 1) | | 0.38 | 0.55 | Ω |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ ≥ 50V, $I_D$ = 5.2A (Note 1) | 5.8 | 8.9 | | S |
| Turn-On Delay Time | $t_{DLY(ON)}$ | $V_{DD}$ = 200V, $I_D$ ≈ 10A, $R_{GS}$ = 9.1Ω, $R_L$ = 20Ω, $V_{GS}$ = 10V MOSFET Switching Times are Essentially Independent of Operating Temperature | | 65 | 75 | ns |
| Rise Time | $t_R$ | | | 130 | 145 | ns |
| Turn-Off Delay Time | $t_{DLY(OFF)}$ | | | 240 | 260 | ns |
| Fall Time | $t_F$ | | | 145 | 155 | ns |
| Total Gate Charge (Gate to Source + Gate to Drain) | $Q_{G(TOT)}$ | $V_{GS}$ = 10V, $I_D$ = 10A, $I_{G(REF)}$ = 1.5mA, $V_{DS}$ = 0.8 x Rated $BV_{DSS}$ Gate Charge is Essentially Independent of Operating Temperature | | 138 | | nC |
| Gate to Source Charge | $Q_{GS}$ | | | 35 | | nC |
| Gate to Drain “Miller” Charge | $Q_{GD}$ | | | 35 | | nC |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0V, $V_{DS}$ =25V, f = 1.0MHz | | 1170 | | pF |
| Output Capacitance | $C_{OSS}$ | | | 160 | | pF |
| Reverse - Transfer Capacitance | $C_{RSS}$ | | | 26 | | pF |
| Internal Drain Inductance | $L_D$ | Measured From the Contact Screw on Tab to Center of Die; Modified MOSFET Symbol Showing the Internal Devices Inductances | | 3.5 | | nH |
| | | Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die | | 4.5 | | nH |
| Internal Source Inductance | $L_S$ | Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad | | 7.5 | | nH |
| **SOURCE TO DRAIN DIODE SPECIFICATIONS** | | | | | | |
| Source to Drain Diode Voltage | $V_{SD}$ | $T_J$ = 25°C, $I_{SD}$ = 10A, $V_{GS}$ = 0V (Note 1) | | | 2.0 | V |
| Continuous Source to Drain Current | $I_S$ | Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode | | | 10 | A |
| Pulse Source to Drain Current (Note 2) | $I_{SM}$ | | | | 40 | A |
| Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25°C, $I_{SD}$ = 10A, $dI_{SD}/dt$ = 100A/μs | 170 | 390 | 790 | ns |
| Reverse Recovery Charge | $Q_{RR}$ | $T_J$ = 25°C, $I_{SD}$ = 10A, $dI_{SD}/dt$ = 100A/μs | 1.6 | 4.5 | 8.2 | μC |



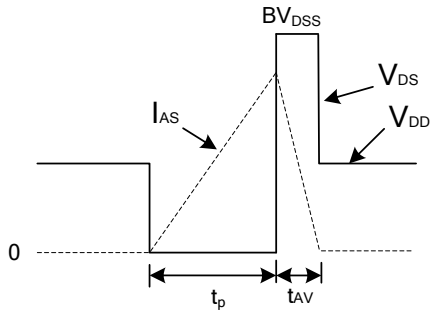




Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle≤2%.
2. Repetitive rating: Pulse width limited by maximum junction temperature.
3. $V_{DD}$=50V, starting $T_J$ =25°C, L=9.1mH, $R_G$=25Ω, peak $I_{AS}$ = 10A

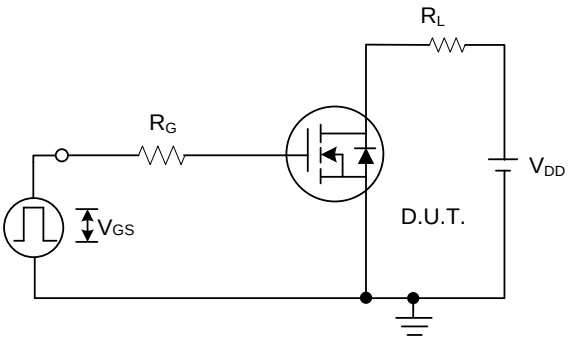
## ■ TEST CIRCUITS AND WAVEFORMS



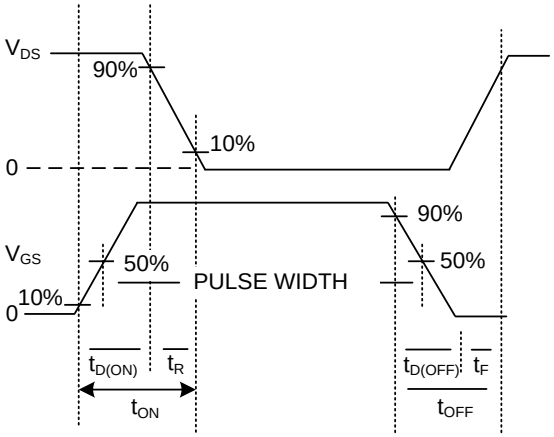

Unclamped Energy Test Circuit



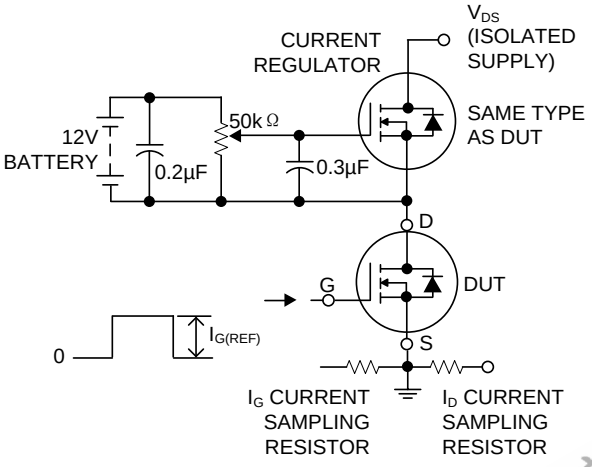

Unclamped Energy Waveforms



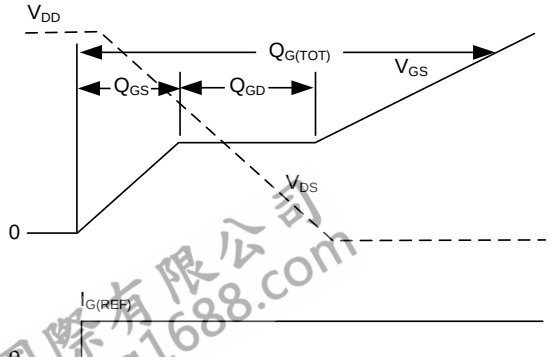

Switching Time Test Circuit




Resistive Switching Waveforms



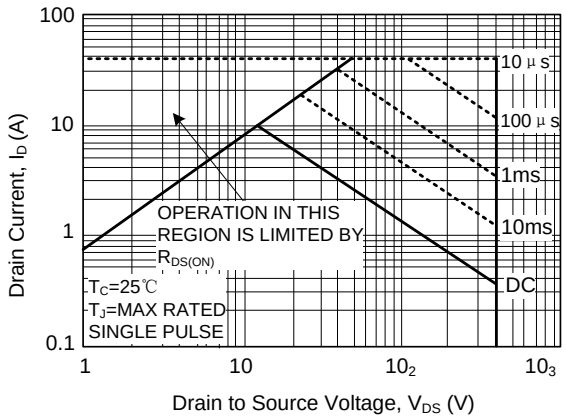

Gate Charge Test Circuit



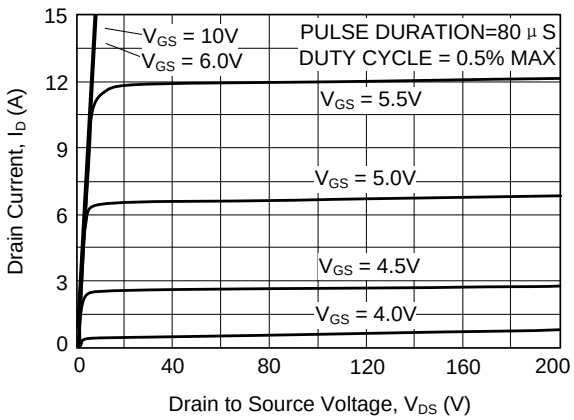

Gate Charge Waveforms

## ■ TYPICAL PERFORMANCE CUVES

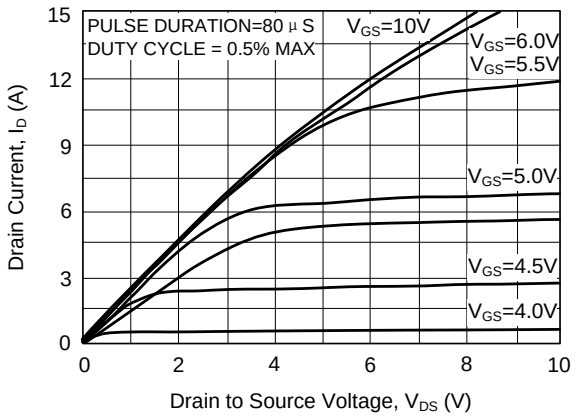
Forward Bias Safe Operating Area



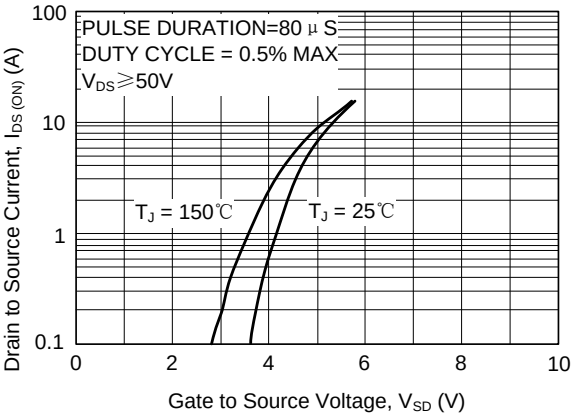

Output Characteristics



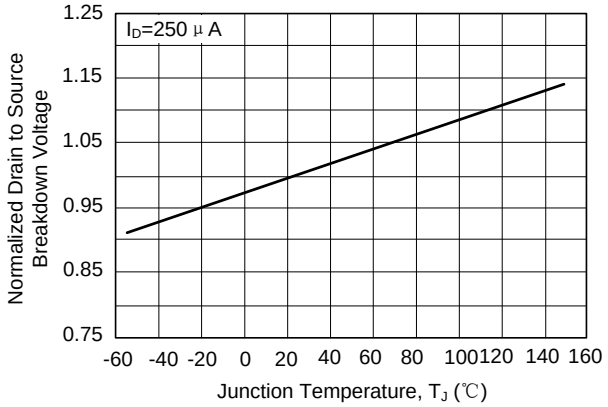

Saturation Characteristics



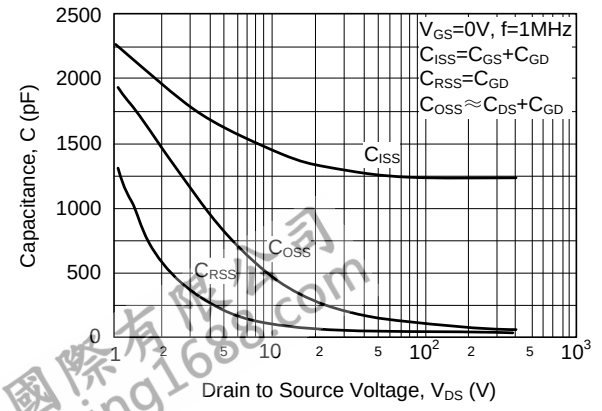

Transfer Characteristics




Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

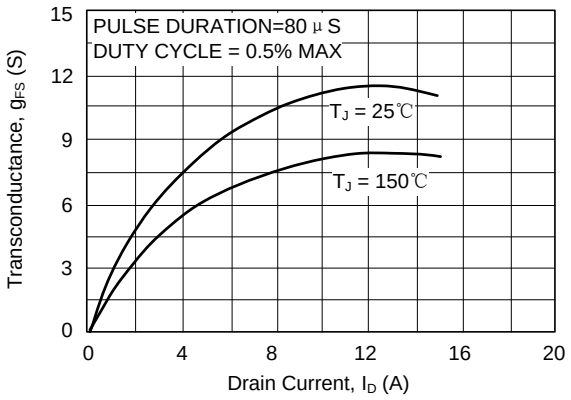



Capacitance vs. Drain to Source Voltage

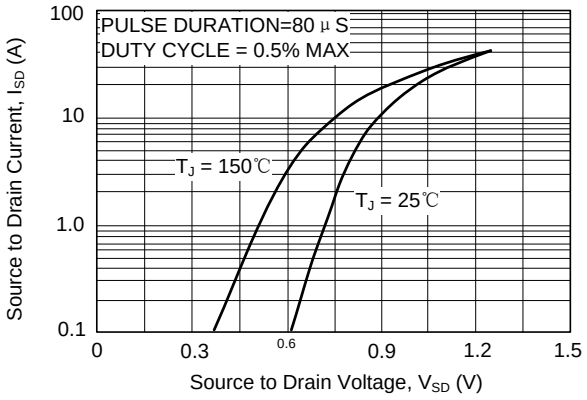


## ■ TYPICAL PERFORMANCE CUVES (Cont.)

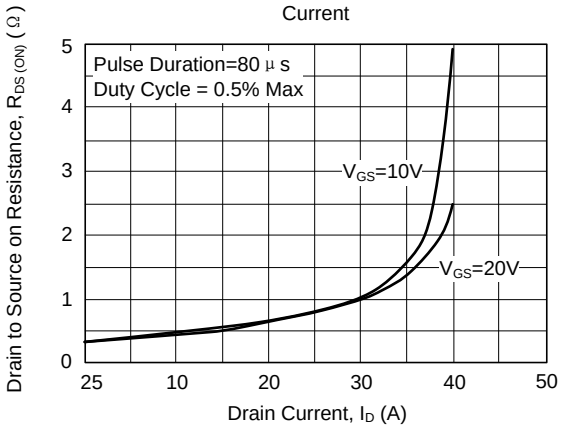
Transconduce vs. Drain Current




Source to Drain Diode Voltage




Drain to Source on Resistance vs. Voltage and Drain Current




Gate to Source Voltage vs. Gate Charge