



UF7832

Preliminary

Power MOSFET

20A, 30V N-CHANNEL POWER MOSFET

DESCRIPTION

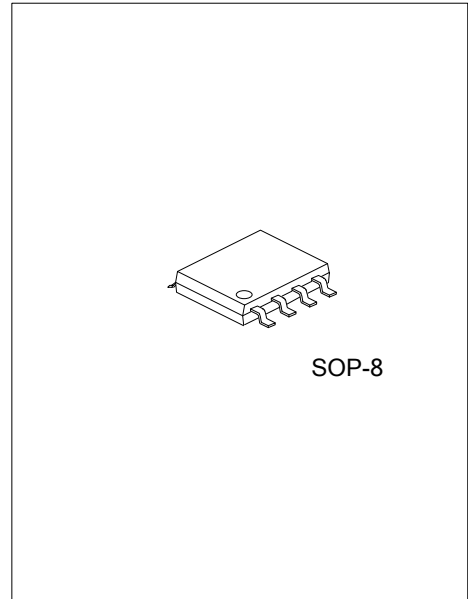
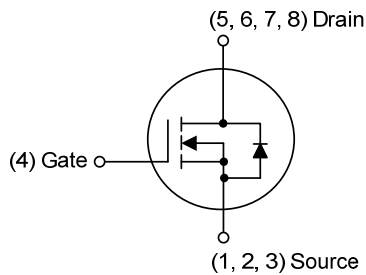
The UTC **UF7832** is an N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

The UTC **UF7832** is suitable for high frequency DC-DC converters with synchronous rectification applications.

FEATURES

- * $R_{DS(ON)} < 4.0m\Omega @ V_{GS}=10V, I_D=10A$
- * $R_{DS(ON)} < 5.5m\Omega @ V_{GS}=4.5V, I_D=16A$
- * High Power and Current Handling Capability
- * High Cell Density Trench Technology

SYMBOL



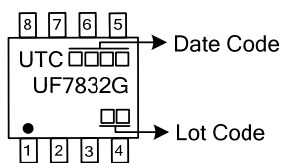
ORDERING INFORMATION

Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UF7832G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

<p>UF7832G-S08-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8</p> <p>(3) G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	20	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	80	A
Avalanche Current (Note 3)		I_{AR}	16	A
Avalanche energy	Single Pulsed (Note 3)	E_{AS}	256	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.0	V/ns
Power Dissipation		P_D	3.5	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=2.0\text{mH}$, $I_{AS}=16\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 20\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	50	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	35.7	$^\circ\text{C}/\text{W}$

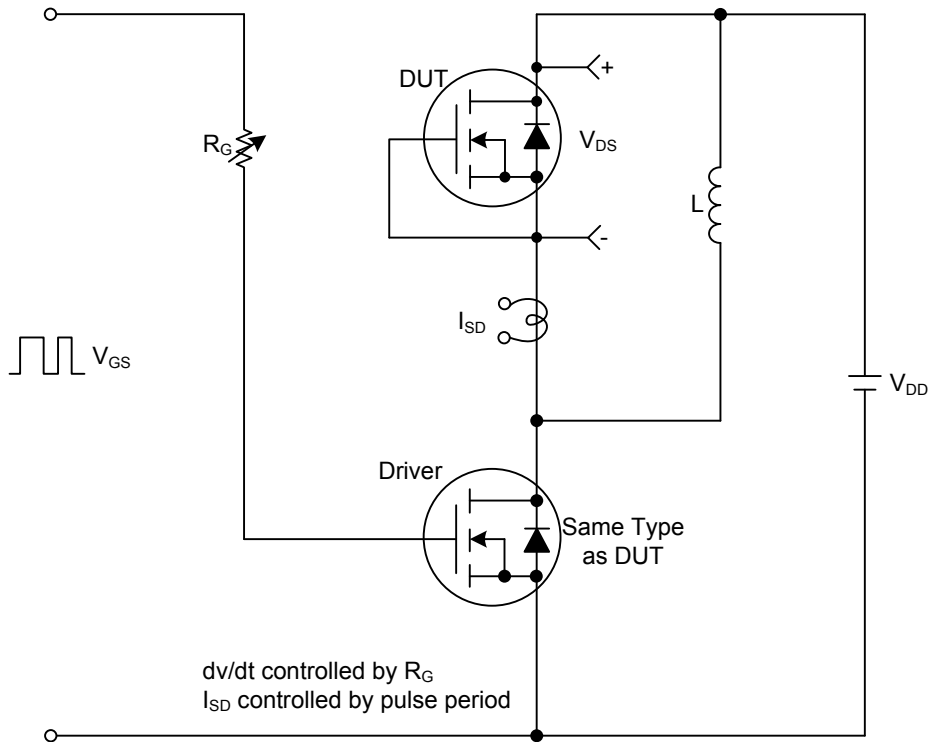
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	Forward			100	nA
		Reverse	$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$		-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		2.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=20\text{A}$			4.0	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=16\text{A}$			5.5	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1\text{MHz}$		4150		pF
Output Capacitance	C_{OSS}			760		pF
Reverse Transfer Capacitance	C_{RSS}			700		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$, $I_G=100\mu\text{A}$ (Note 1, 2)		34		nC
Gate to Source Charge	Q_{GS}			8.6		nC
Gate to Drain Charge	Q_{GD}			12		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		88		ns
Rise Time	t_R			352		ns
Turn-off Delay Time	$t_{D(OFF)}$			1620		ns
Fall-Time	t_F			1060		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				20	A
Maximum Body-Diode Pulsed Current	I_{SM}				80	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=16\text{A}$, $V_{GS}=0\text{V}$			1.0	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_F=20\text{A}$, $V_{GS}=0\text{V}$,		500		nS
Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$		1.5		μC

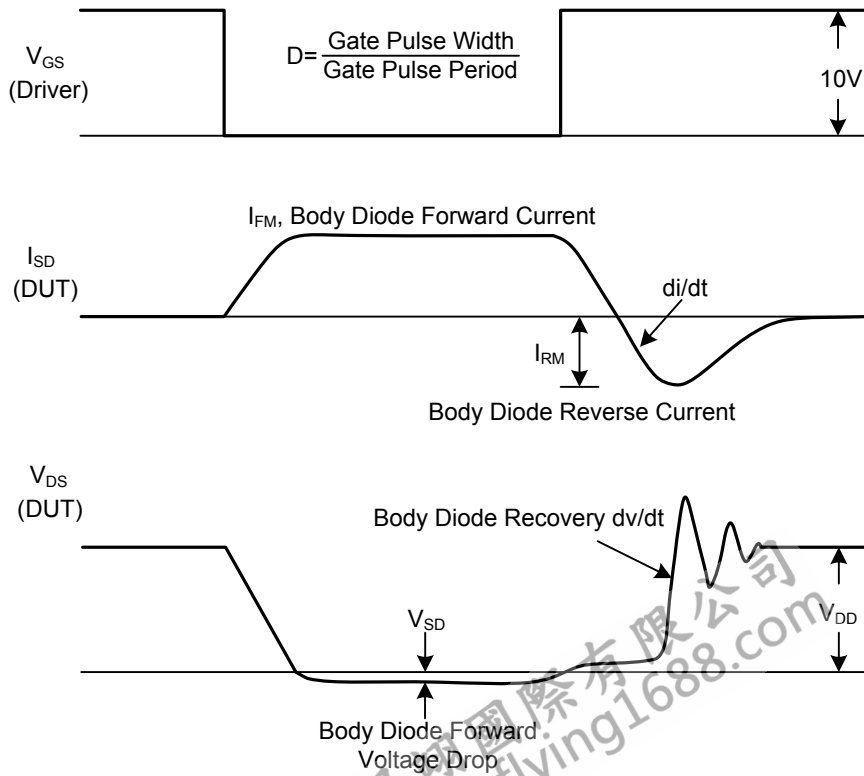
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

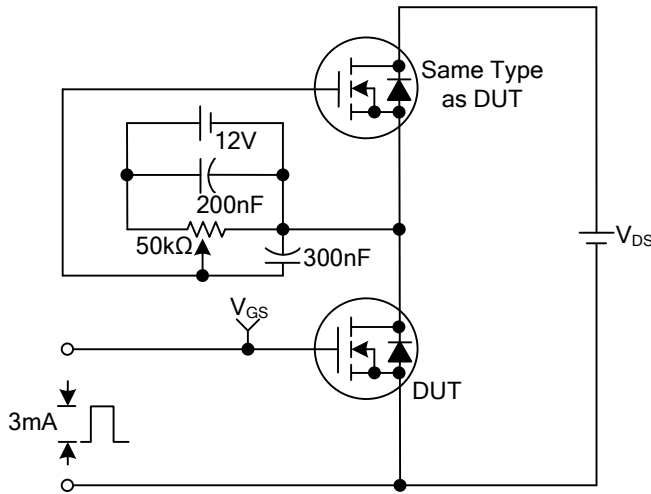
■ TEST CIRCUITS AND WAVEFORMS



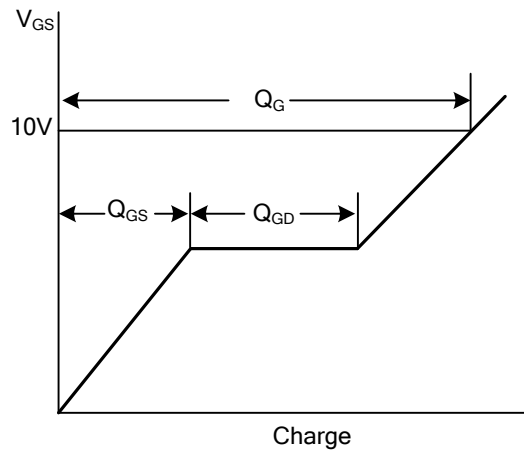
Peak Diode Recovery dv/dt Test Circuit & Waveforms



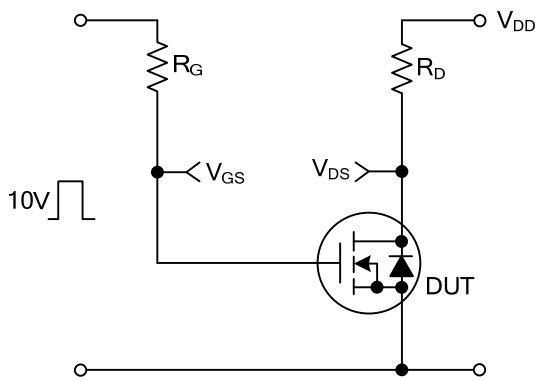
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



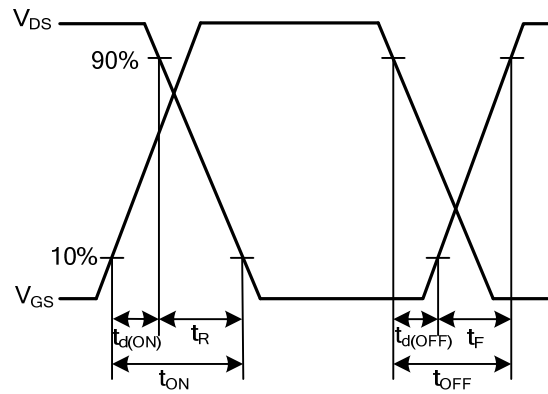
Gate Charge Test Circuit



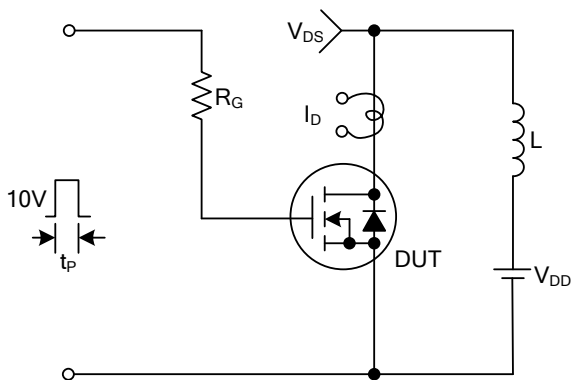
Gate Charge Waveforms



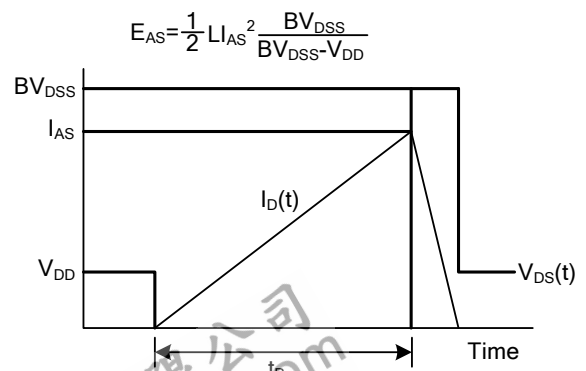
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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