



UF830K-TA

Preliminary

Power MOSFET

4.5A, 500V, 1.5Ω, N-CHANNEL POWER MOSFET

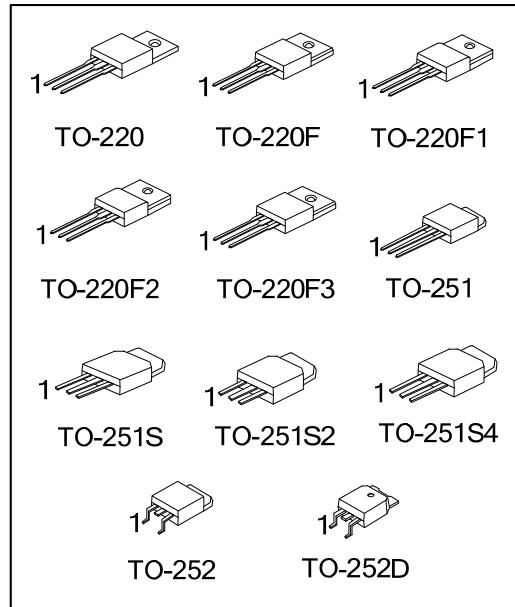
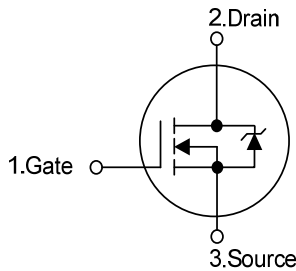
DESCRIPTION

The UTC UF830K-TA is a N-Channel enhancement mode silicon gate power MOSFET is designed high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

FEATURES

- * $R_{DS(ON)} < 1.8\Omega @ V_{GS} = 10V, I_D = 2.5 A$
- * Single Pulse Avalanche Energy Rated
- * Rugged- SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

SYMBOL



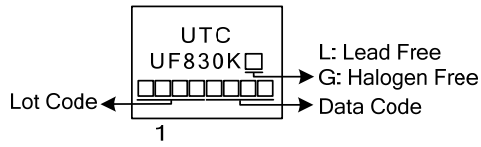
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF830KL-TA3-T	UF830KG-TA3-T	TO-220	G	D	S	Tube
UF830KL-TF3-T	UF830KG-TF3-T	TO-220F	G	D	S	Tube
UF830KL-TF1-T	UF830KG-TF1-T	TO-220F1	G	D	S	Tube
UF830KL-TF2-T	UF830KG-TF2-T	TO-220F2	G	D	S	Tube
UF830KL-TF3T-T	UF830KG-TF3T-T	TO-220F3	G	D	S	Tube
UF830KL-TM3-T	UF830KG-TM3-T	TO-251	G	D	S	Tube
UF830KL-TMS-T	UF830KG-TMS-T	TO-251S	G	D	S	Tube
UF830KL-TMS2-T	UF830KG-TMS2-T	TO-251S2	G	D	S	Tube
UF830KL-TMS4-T	UF830KG-TMS4-T	TO-251S4	G	D	S	Tube
UF830KL-TN3-R	UF830KG-TN3-R	TO-252	G	D	S	Tape Reel
UF830KL-TND-R	UF830KG-TND-R	TO-252D	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UF830KL-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1, TF2: TO-220F2, TF3T: TO-220F3, TM3: TO-251, TMS: TO-251S, TMS2: TO-251S2, TMS4: TO-251S4, TN3: TO-252, TND: TO-252D</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



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■ **ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, Unless Otherwise Specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage ($T_J=25^\circ\text{C} \sim 125^\circ\text{C}$)		V_{DS}	500	V
Drain to Gate Voltage ($R_G=20\text{k}\Omega$, $T_J=25^\circ\text{C} \sim 125^\circ\text{C}$)		V_{DGR}	500	V
Gate to Source Voltage		V_{GS}	± 30	V
Drain Current	Continuous	I_D	4.5	A
	Pulsed	I_{DM}	18	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	2	V/ns
Power Dissipation ($T_C = 25^\circ\text{C}$)	TO-220	P_D	73	W
	TO-220F/TO-220F1 TO-220F3		38	W
	TO-220F2		40	W
	TO-251/TO-251S TO-251S2/ TO-251S4 TO-252/TO-252D		46	W
Single Pulse Avalanche Energy Rating (Note 2)		E_{AS}	80	mJ
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. $L = 8\text{mH}$, $I_{AS} = 4.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

3. $I_{SD} \leq 4.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F TO-220F1/TO-220F2 TO-220F3	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
	TO-251/TO-251S TO-251S2/ TO-251S4 TO-252/TO-252D		100.3	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	1.71	$^\circ\text{C}/\text{W}$
	TO-220F/TO-220F1 TO-220F3		3.31	$^\circ\text{C}/\text{W}$
	TO-220F2		3.125	$^\circ\text{C}/\text{W}$
	TO-251/TO-251S TO-251S2/ TO-251S4 TO-252/TO-252D		2.7	$^\circ\text{C}/\text{W}$

■ **ELECTRICAL SPECIFICATIONS** ($T_A = 25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	500			V
On-State Drain Current (Note 1)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times R_{DS(ON)MAX}$, $V_{GS} = 10\text{V}$	4.5			A
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$			25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$			250	μA
		$V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$				
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$I_D = 2.5\text{A}$, $V_{GS} = 10\text{V}$ (Note 2)			1.8	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$		260		pF
Output Capacitance	C_{OSS}			56		pF
Reverse Transfer Capacitance	C_{RSS}			7		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS} = 10\text{V}$, $I_D = 1.3\text{A}$, $V_{DD} = 50\text{V}$ $I_G = 100\mu\text{A}$ (Note 3)		45		nC
Gate-Source Charge	Q_{GS}			4		nC
Gate-Drain Charge	Q_{GD}			4		nC
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$, $R_G = 25\Omega$ (Note 2)		36		ns
Turn-On Rise Time	t_R			29		ns
Turn-Off Delay Time	$t_{D(OFF)}$			110		ns
Turn-Off Fall Time	t_F			29		ns
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Source to Drain Diode Voltage ($T_J = 25^\circ\text{C}$)	V_{SD}	$I_{SD} = 4.4\text{A}$, $V_{GS} = 0\text{V}$ (Note 1)			1.6	V
Continuous Source to Drain Current	I_S	(Note 4)			4.5	A
Pulse Source to Drain Current	I_{SD}					18
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{V}$, $I_S = 4.5\text{A}$,		450		nS
Reverse Recovery Charge	Q_{RR}	$dI_F / dt = 100\text{A}/\mu\text{s}$ (Note 1)		3		μC

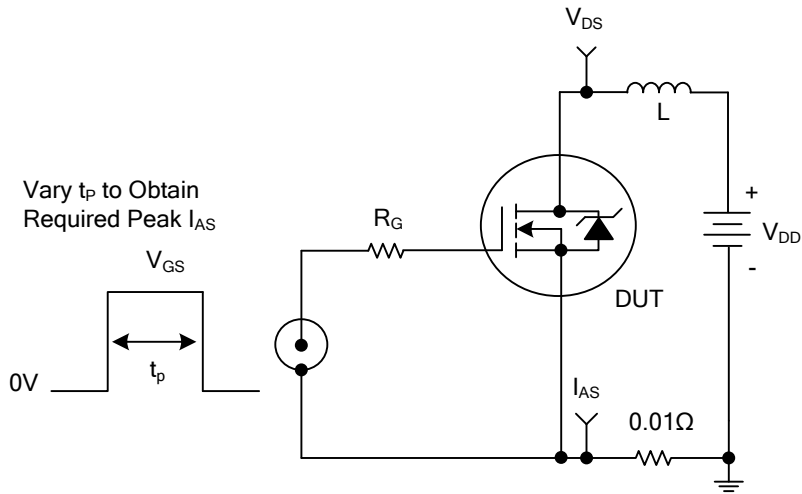
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

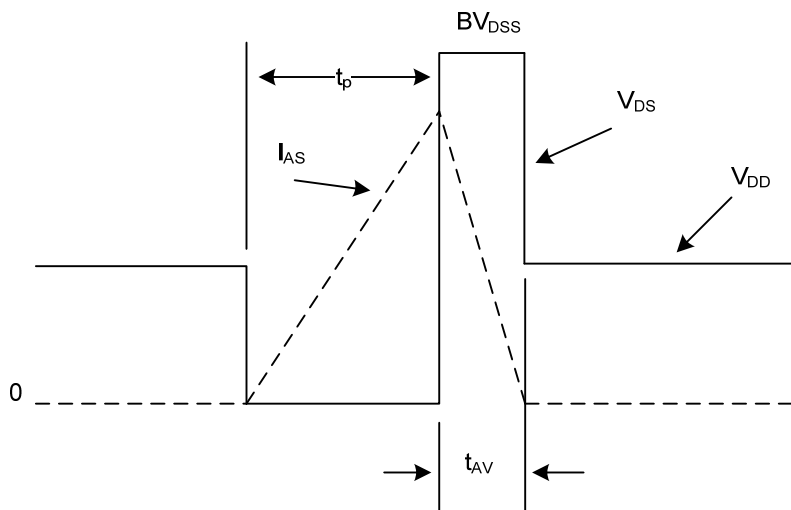
3. Gate Charge is Essentially Independent of Operating Temperature.

4. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.

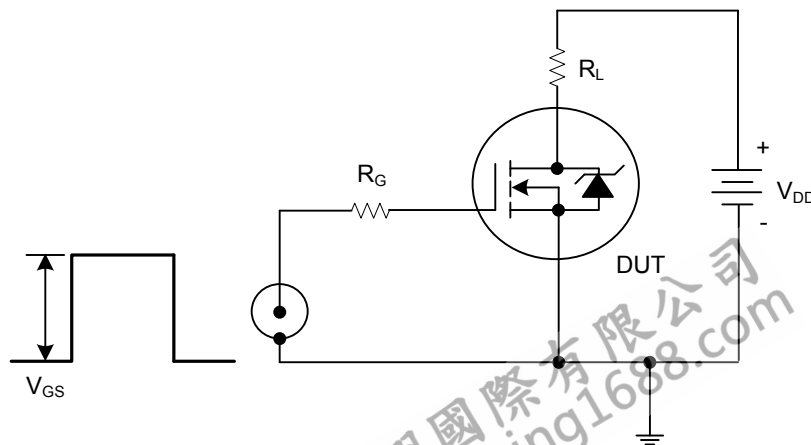
■ TEST CIRCUITS AND WAVEFORMS



Unclamped Energy Test Circuit

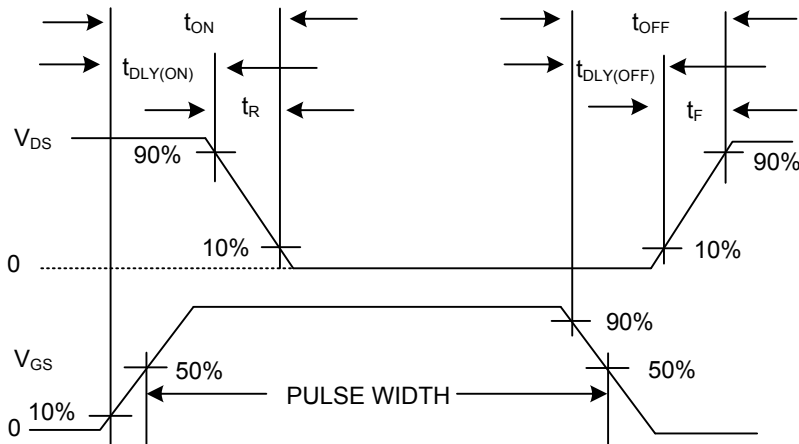


Unclamped Energy Waveforms

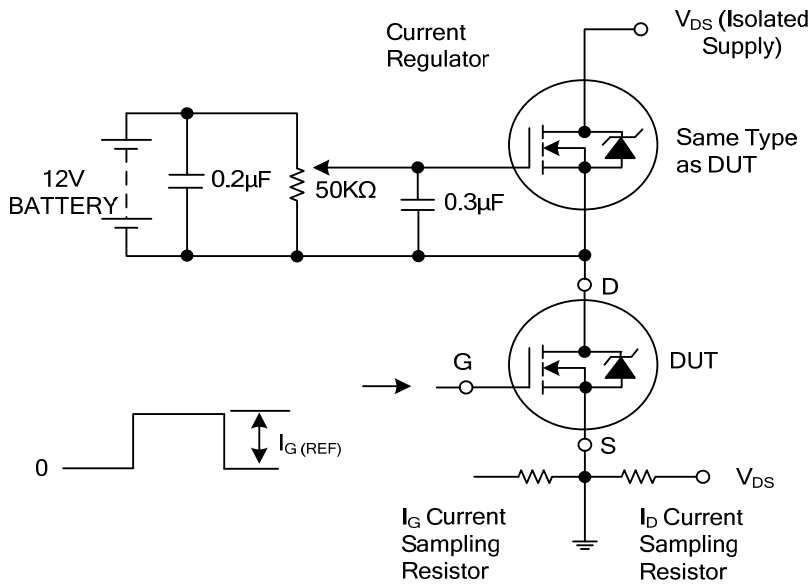


Switching Time Test Circuit

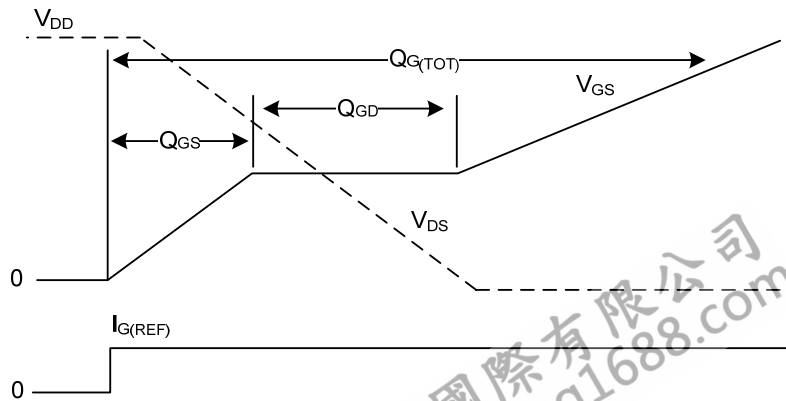
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



Resistive Switching Waveforms



Gate Charge Test Circuit



Gate Charge Waveforms

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