



UF830K-TC

Power MOSFET

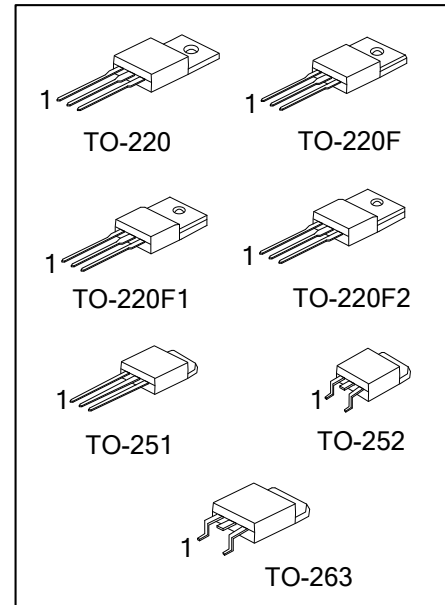
4.5A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

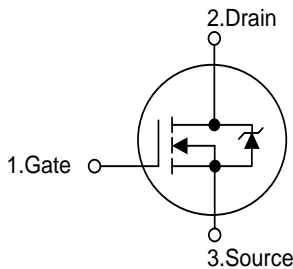
The UTC UF830K-TC is a N-Channel enhancement mode silicon gate power MOSFET is designed high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

FEATURES

- * $R_{DS(ON)} \leq 1.65 \Omega @ V_{GS}=10V, I_D=2.5A$
- * Single Pulse Avalanche Energy Rated
- * Rugged- SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance



SYMBOL



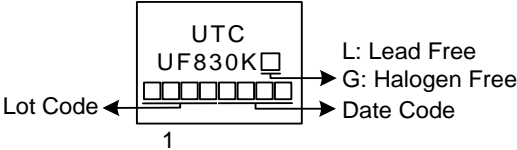
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF830KL-TA3-T	UF830KG-TA3-T	TO-220	G	D	S	Tube
UF830KL-TF1-T	UF830KG-TF1-T	TO-220F1	G	D	S	Tube
UF830KL-TF2-T	UF830KG-TF2-T	TO-220F2	G	D	S	Tube
UF830KL-TF3-T	UF830KG-TF3-T	TO-220F	G	D	S	Tube
UF830KL-TM3-T	UF830KG-TM3-T	TO-251	G	D	S	Tube
UF830KL-TN3-R	UF830KG-TN3-R	TO-252	G	D	S	Tape Reel
UF830KL-TQ2-T	UF830KG-TQ2-T	TO-263	G	D	S	Tube
UF830KL-TQ2-R	UF830KG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UF830KG-TA3-T</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) T: Tube, R: Tape Reel (2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1, TF2: TO-220F2, TM3: TO-251, TN3: TO-252, TQ2: TO-263 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



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■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless Otherwise Specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T _J =25°C ~125°C)		V _{DS}	500	V
Drain to Gate Voltage (R _G =20kΩ, T _J =25°C ~125°C)		V _{DGR}	500	V
Gate to Source Voltage		V _{GS}	±30	V
Drain Current	Continuous	I _D	4.5	A
	Pulsed	I _{DM}	18	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	2	V/ns
Power Dissipation	TO-220/TO-263	P _D	73	W
	TO-220F/TO-220F1		38	W
	TO-220F2		40	W
	TO-251/TO-252		46	W
Single Pulse Avalanche Energy Rating (Note 2)		E _{AS}	110	mJ
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. L = 10mH, I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C

3. I_{SD} ≤ 4.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient	TO-220/TO-220F	θ _{JA}	62.5	°C/W
	TO-220F1/TO-220F2			
	TO-263			
	TO-251/TO-252		100.3	
Junction to Case	TO-220/TO-263	θ _{JC}	1.71	°C/W
	TO-220F/TO-220F1		3.31	
	TO-220F2		3.125	
	TO-251/TO-252		2.7	

■ **ELECTRICAL SPECIFICATIONS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=\text{Rated } BV_{DSS}$, $V_{GS}=0\text{V}$			25	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$I_D=2.5\text{A}$, $V_{GS}=10\text{V}$			1.65	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		267		pF
Output Capacitance	C_{OSS}			64		pF
Reverse Transfer Capacitance	C_{RSS}			7		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$ $I_G=100\mu\text{A}$ (Note 1, 2)		41		nC
Gate-Source Charge	Q_{GS}			4		nC
Gate-Drain Charge	Q_{GD}			4		nC
Turn-On Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		44		ns
Turn-On Rise Time	t_R			49		ns
Turn-Off Delay Time	$t_{D(OFF)}$			268		ns
Turn-Off Fall Time	t_F			79		ns
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Continuous Source to Drain Current	I_S	(Note 4)			4.5	A
Pulse Source to Drain Current	I_{SD}				18	A
Source to Drain Diode Voltage (Note 1)	V_{SD}	$I_{SD}=4.5\text{A}$, $V_{GS}=0\text{V}$			1.6	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_{SD}=4.5\text{A}$, $V_{GS}=0\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$		250		nS
Reverse Recovery Charge	Q_{rr}			1.0		μC

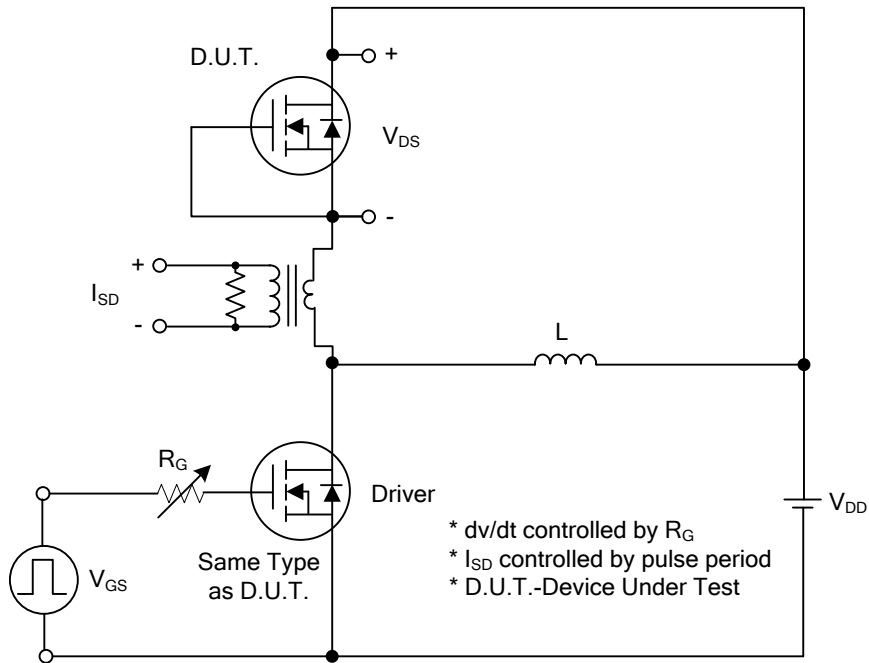
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

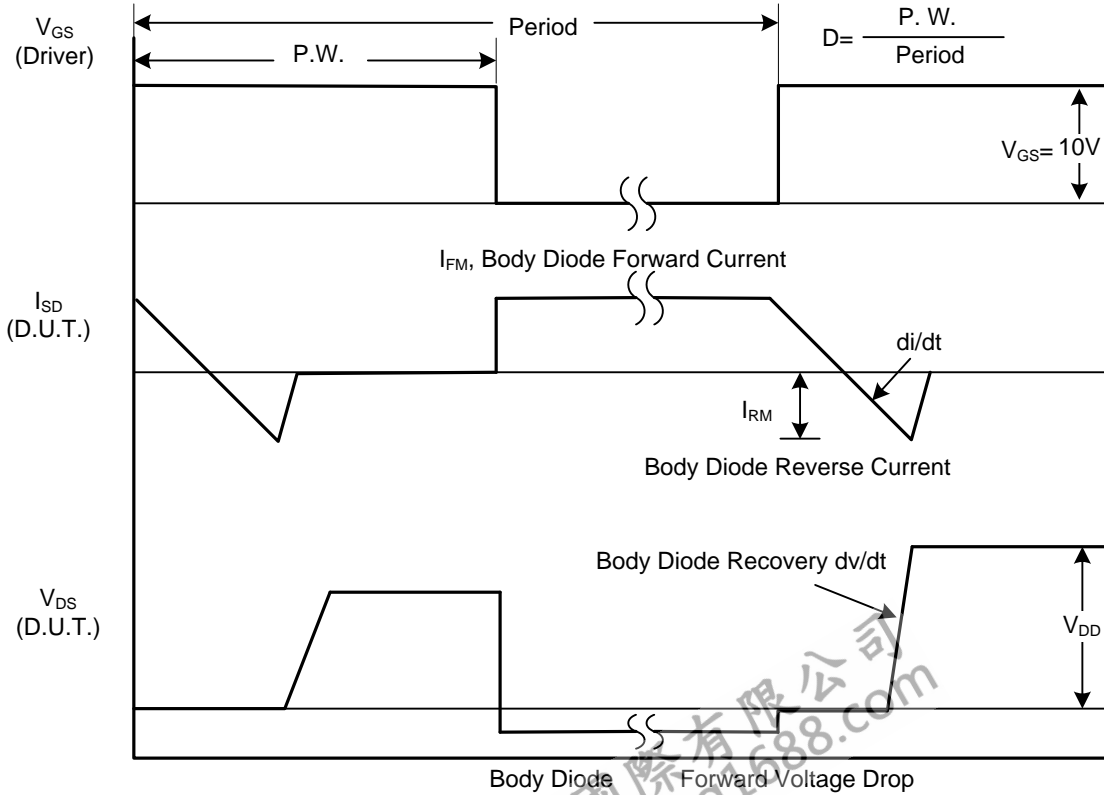
3. Gate Charge is Essentially Independent of Operating Temperature.

4. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.

TEST CIRCUITS AND WAVEFORMS

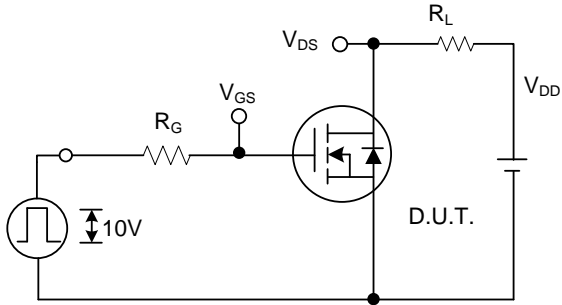


Peak Diode Recovery dv/dt Test Circuit

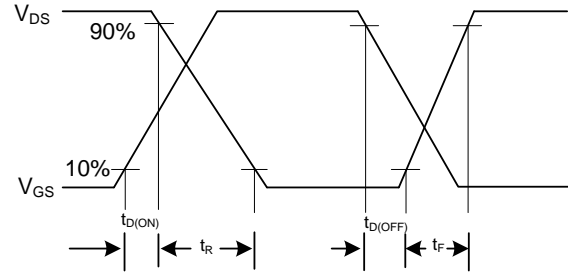


Peak Diode Recovery dv/dt Waveforms

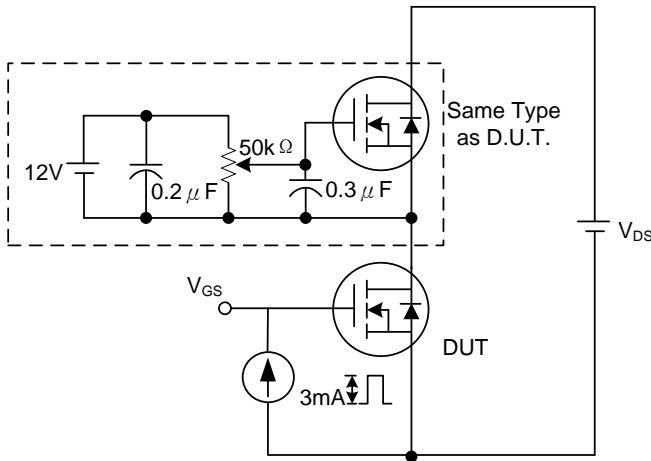
TEST CIRCUITS AND WAVEFORMS (Cont.)



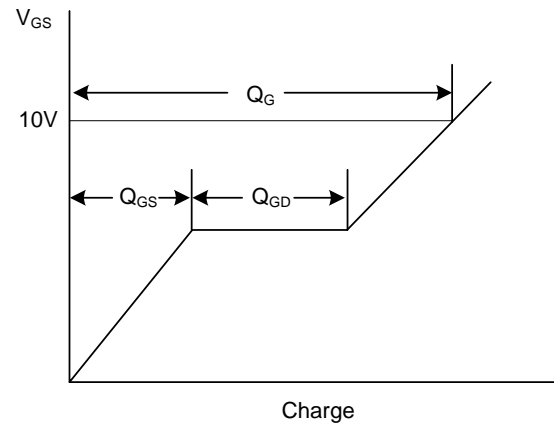
Switching Test Circuit



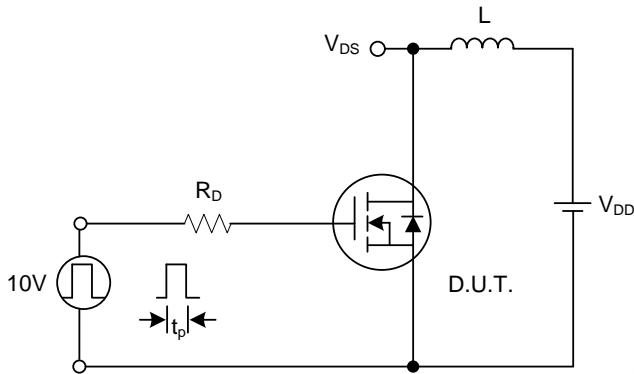
Switching Waveforms



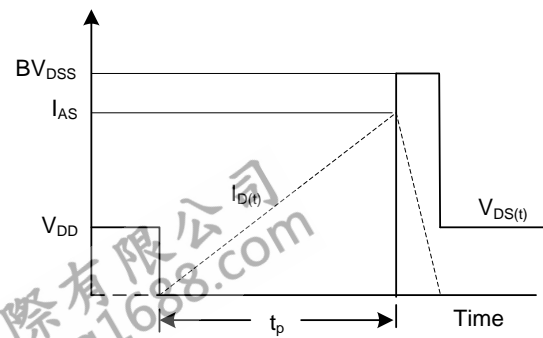
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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