



UF830K

Preliminary

Power MOSFET

**4.5A, 500V, 1.5Ω, N-CHANNEL POWER MOSFET**

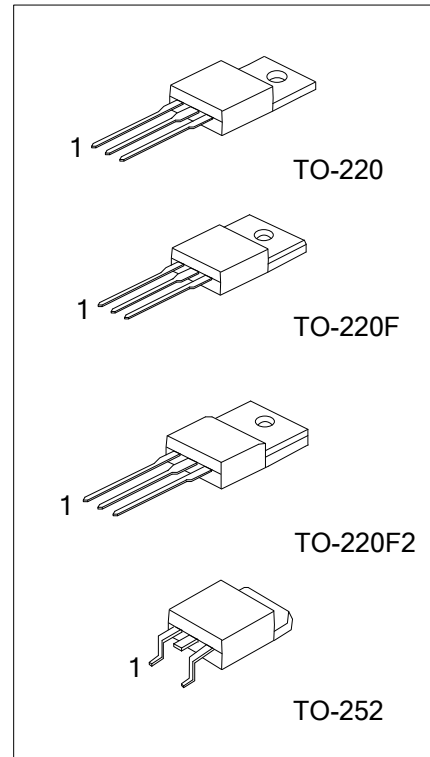
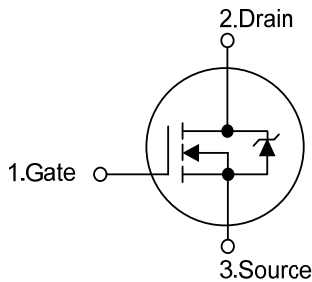
■ **DESCRIPTION**

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ **FEATURES**

- \*  $R_{DS(ON)} < 1.5\Omega @ I_D = 2.5A$
- \* Single Pulse Avalanche Energy Rated
- \* Rugged- SOA is Power Dissipation Limited
- \* Fast Switching Speeds
- \* Linear Transfer Characteristics
- \* High Input Impedance

■ **SYMBOL**



■ **ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF830KL-TA3-T	UF830KG-TA3-T	TO-220	G	D	S	Tube
UF830KL-TF3-T	UF830KG-TF3-T	TO-220F	G	D	S	Tube
UF830KL-TF2-T	UF830KG-TF2-T	TO-220F2	G	D	S	Tube
UF830KL-TN3-R	UF830KG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UF830KL-TA3-T</p>	<p>(1) T: Tube, R: Tape Reel                  (2) TA3: TO-220, TF3: TO-220F, TF2: TO-220F2, TN3: TO-252                  (3) L: Lead Free, G: Halogen Free</p>
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■ **MARKING INFORMATION**

PACKAGE	MARKING
TO-220 TO-220F TO-220F2 TO-252	<p>UTC UF830K Lot Code Data Code</p> <p>L: Lead Free G: Halogen Free</p>

### ■ ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, Unless Otherwise Specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T <sub>J</sub> =25°C ~125°C)		V <sub>DS</sub>	500	V
Drain to Gate Voltage (R <sub>GS</sub> =20kΩ, T <sub>J</sub> =25°C ~125°C)		V <sub>DGR</sub>	500	V
Gate to Source Voltage		V <sub>GS</sub>	±30	V
Drain Current	Continuous	I <sub>D</sub>	4.5	A
	Pulsed	I <sub>DM</sub>	18	A
Power Dissipation (T <sub>C</sub> = 25°C)	TO-220	P <sub>D</sub>	73	W
	TO-220F		38	W
	TO-220F2		40	W
	TO-252		50	W
Single Pulse Avalanche Energy Rating (Note 2)		E <sub>AS</sub>	300	mJ
Junction Temperature		T <sub>J</sub>	+150	°C
Storage Temperature		T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=25mH, R<sub>G</sub>=25Ω, peak I<sub>AS</sub>=4.5A

### ■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F	θ <sub>JA</sub>	62.5	°C/W
	TO-220F2			
	TO-252			
Junction to Case	TO-220	θ <sub>Jc</sub>	1.71	°C/W
	TO-220F		3.31	
	TO-220F2		3.125	
	TO-252		2.5	°C/W

### ■ ELECTRICAL SPECIFICATIONS (T<sub>A</sub> =25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	500			V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	2.0		4.0	V
On-State Drain Current (Note 1)	I <sub>D(ON)</sub>	V <sub>DS</sub> >I <sub>D(ON)</sub> ×R <sub>DS(ON)MAX</sub> , V <sub>GS</sub> =10V	4.5			A
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = Rated BV <sub>DSS</sub> , V <sub>GS</sub> =0V			25	μA
		V <sub>DS</sub> =0.8×Rated BV <sub>DSS</sub> V <sub>GS</sub> =0V, T <sub>J</sub> = 125°C			250	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V			±100	nA
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	I <sub>D</sub> =2.5A, V <sub>GS</sub> =10V (Note 2)		1.23	1.5	Ω
Forward Transconductance (Note 1)	g <sub>FS</sub>	V <sub>DS</sub> ≥10V, I <sub>D</sub> =2.7A	2.5	4.2		S
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> ≈0.5A R <sub>GS</sub> =12Ω, R <sub>L</sub> =54Ω (Note 2)		48	60	ns
Turn-On Rise Time	t <sub>r</sub>			48	60	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			40	53	ns
Turn-Off Fall Time	t <sub>f</sub>			44	60	ns
Total Gate Charge	Q <sub>G</sub>		V <sub>GS</sub> =10V, I <sub>D</sub> =1.3A		14	32
Gate-Source Charge	Q <sub>GS</sub>	V <sub>DS</sub> =50V		5.4		nC
Gate-Drain Charge	Q <sub>GD</sub>	I <sub>G(REF)</sub> =100μA (Note 3)		6		nC
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz		590		pF
Output Capacitance	C <sub>OSS</sub>			80		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			15		pF

Notes: 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.

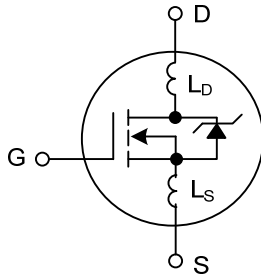
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

3. Gate Charge is Essentially Independent of Operating Temperature.

INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Internal Drain Inductance</b>					
Measured from the contact screw on tab to center of die	$L_D$		3.5		nH
Measured from the drain lead(6mm from package) to center of die			4.5		nH
<b>Internal Source Inductance</b>					
Measured from the source lead(6mm from header) to source bond pad	$L_S$		7.5		nH

Remark: Modified MOSFET symbol showing the internal devices inductances as below.

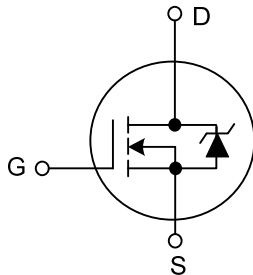


SOURCE TO DRAIN DIODE SPECIFICATIONS

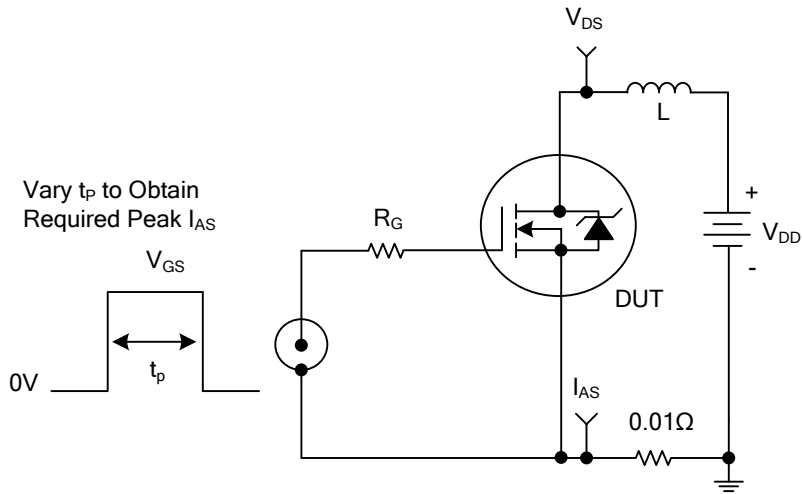
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage	$V_{SD}$	$T_J=25^{\circ}C, I_{SD}=4.5A, V_{GS}=0V$ (Note 1)			1.6	V
Continuous Source to Drain Current	$I_{SD}$	(Note 2)			5.5	A
Pulse Source to Drain Current	$I_{SDM}$				18	A
Reverse Recovery Time	$t_{rr}$	$T_J=25^{\circ}C, I_{SD}=4.5A, dI/dt=100A/\mu s$	180	350	760	ns
Reverse Recovery Charge	$Q_{RR}$	$T_J=25^{\circ}C, I_{SD}=4.5A, dI/dt=100A/\mu s$	0.96	2.2	4.3	$\mu C$

Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ .

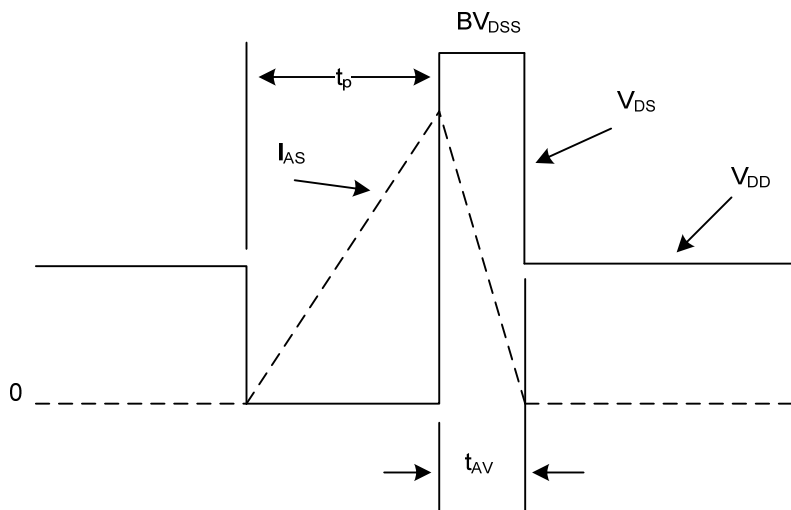
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



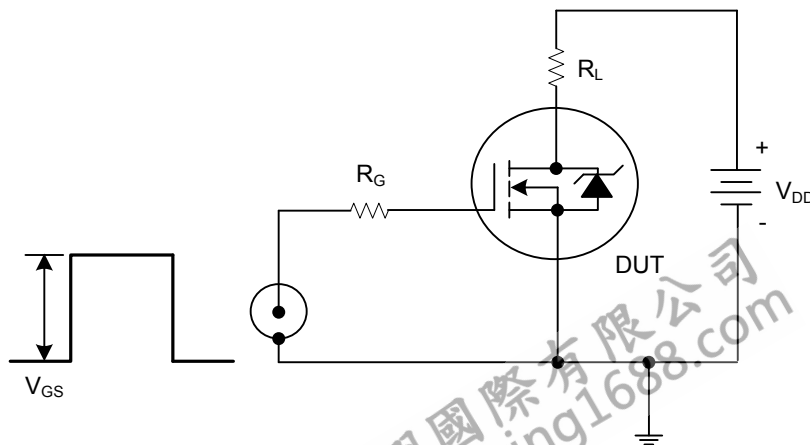
■ TEST CIRCUITS AND WAVEFORMS



Unclamped Energy Test Circuit

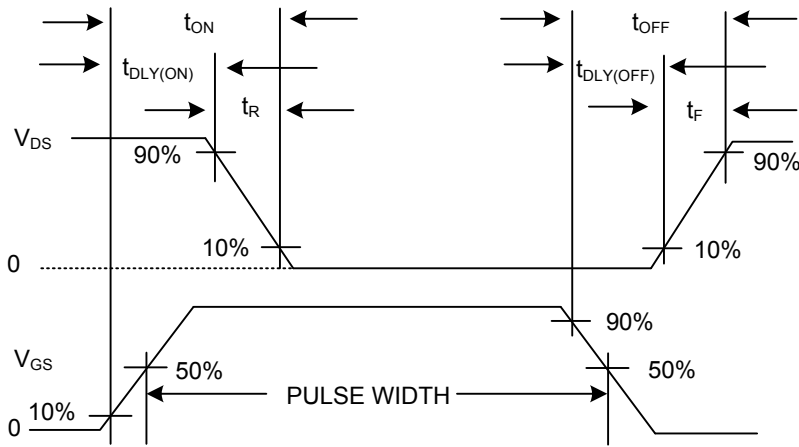


Unclamped Energy Waveforms

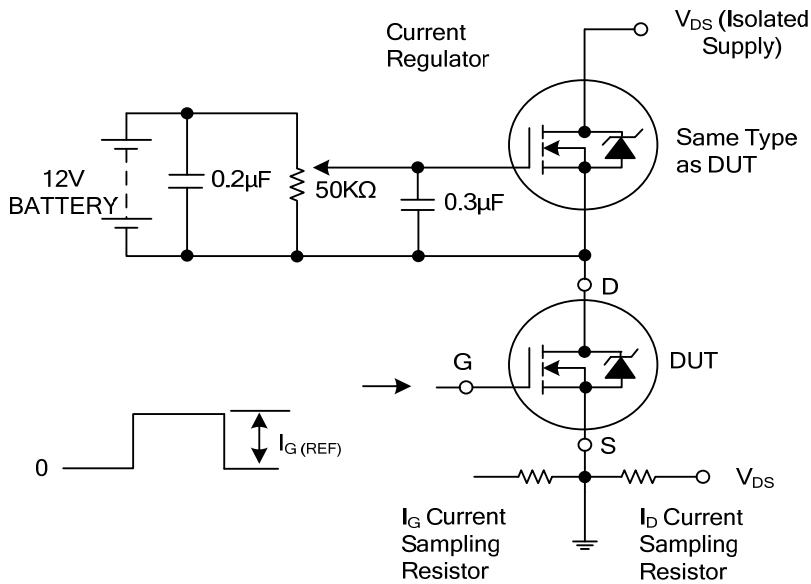


Switching Time Test Circuit

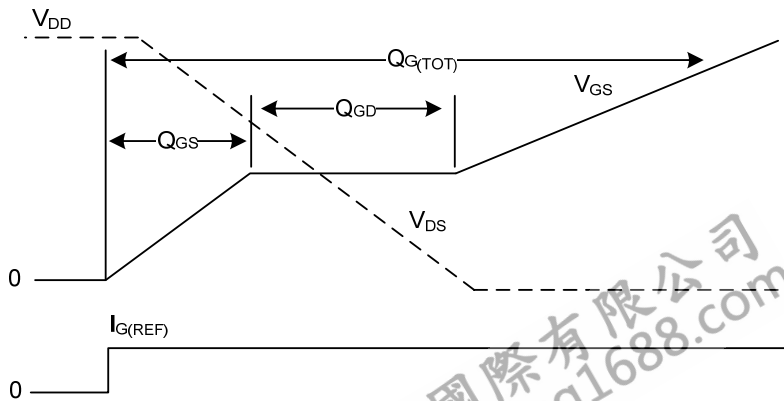
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



Resistive Switching Waveforms



Gate Charge Test Circuit



Gate Charge Waveforms

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