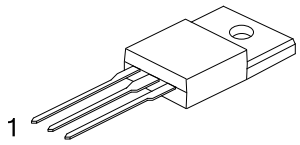
4.5A, 500V, 1.5Ω, N-CHANNEL POWER MOSFET



TO-220F

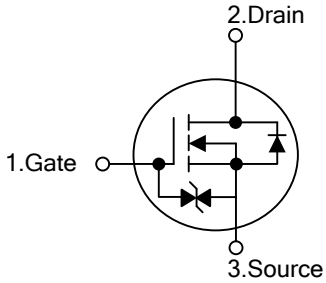
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications, such as switching regulators, switching converters, solenoid, motor drivers and related drivers.

■ FEATURES

* $R_{DS(ON)}$ < 1.5Ω @ I_D=2.5A, V_{GS}=10V
* Single Pulse Avalanche Energy Rated
* Rugged- SOA is Power Dissipation Limited
* Fast Switching Speeds
* Linear Transfer Characteristics
* High Input Impedance
* ESD Protected

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF830ZL-TF3-T	UF830ZG-TF3-T	TO-220F	G	D	S	Tube

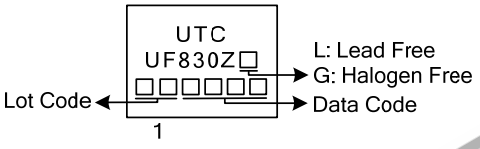
Note: Pin Assignment: G: Gate D: Drain S: Source

UF830ZL-TF3-T

(1)Packing Type
(2)Package Type
(3)Green Package

(1) T: Tube
(2) TF3: TO-220F
(3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless Otherwise Specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T_J=25°C ~125°C)		V_{DS}	500	V
Drain to Gate Voltage (R_{GS}=20kΩ, T_J=25°C ~125°C)		V_{DGR}	500	V
Gate to Source Voltage		V_{GS}	±30	V
Drain Current	Continuous	I_D	4.5	A
	Pulsed	I_{DM}	18	A
Power Dissipation (T_C = 25°C)		P_D	38	W
Single Pulse Avalanche Energy Rating (Note 2)		E_{AS}	300	mJ
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. V_{DD}=50V, starting T_J =25°C, L=25mH, R_G=25Ω, peak I_{AS}=4.5A

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	°C/W
Junction to Case	θ_{JC}	3.31	°C/W

■ ELECTRICAL SPECIFICATIONS (Ta =25°C, unless otherwise specified.)

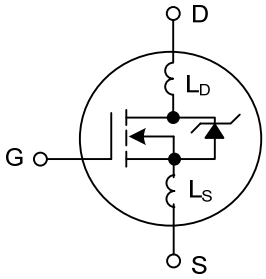
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	500			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D=250μA	2.0		4.0	V
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS}>$I_{D(ON)}$×$R_{DS(ON)MAX}$, V_{GS}=10V	4.5			A
Drain-Source Leakage Current	I_{DSS}	V_{DS}= Rated BV_{DSS}, V_{GS}=0V			25	μA
		V_{DS}=0.8×Rated BV_{DSS} V_{GS}=0V, T_J= 125°C			250	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V			±800	nA
Static Drain-Source On-State Resistance (Note 2)	$R_{DS(ON)}$	I_D=2.5A, V_{GS}=10V		1.3	1.5	Ω
Forward Transconductance (Note 1)	g_{FS}	V_{DS}≥10V, I_D=2.7A	2.5	4.2		S
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=250V, I_D≈4.5A R_{GS}=12Ω, R_L =54Ω (Note 2)		10	17	ns
Turn-On Rise Time	t_R			15	23	ns
Turn-Off Delay Time	$t_{D(OFF)}$			33	53	ns
Turn-Off Fall Time	t_F			16	23	ns
Total Gate Charge	Q_G	V_{GS}=10V, I_D=4.5A V_{DS}=0.8×Rated BV_{DSS} $I_{G(REF)}$=1.5mA (Note 3)		22	32	nC
Gate-Source Charge	Q_{GS}			3.5		nC
Gate-Drain Charge	Q_{GD}			11		nC
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz		600		pF
Output Capacitance	C_{OSS}			100		pF
Reverse Transfer Capacitance	C_{RSS}			20		pF

Notes: 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.
3. Gate Charge is Essentially Independent of Operating Temperature.

■ INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Internal Drain Inductance					
Measured from the contact screw on tab to center of die	L_D		3.5		nH
Measured from the drain lead(6mm from package) to center of die			4.5		nH
Internal Source Inductance					
Measured from the source lead(6mm from header) to source bond pad	L_S		7.5		nH

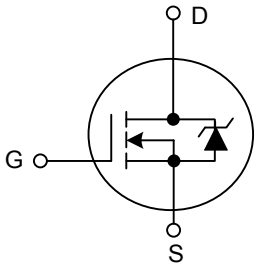
Remark: Modified MOSFET symbol showing the internal devices inductances as below.



■ SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage (Note 1)	V_{SD}	T_J=25°C, I_{SD}=4.5A, V_{GS}=0V			1.6	V
Continuous Source to Drain Current	I_{SD}	Note 2			5.5	A
Pulse Source to Drain Current	I_{SDM}				18	A
Reverse Recovery Time	t_{RR}	T_J=25°C, I_{SD}=4.5A, dI/dt=100A/μs	180	350	760	ns
Reverse Recovery Charge	Q_{RR}	T_J=25°C, I_{SD}=4.5A, dI/dt=100A/μs	0.96	2.2	4.3	μC

NOTE : 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



■ TEST CIRCUITS AND WAVEFORMS

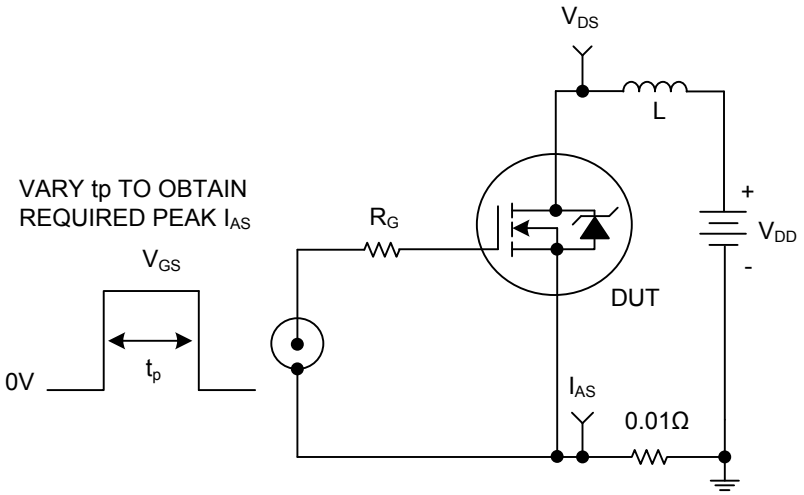


FIG 1. Unclamped Energy Test Circuit

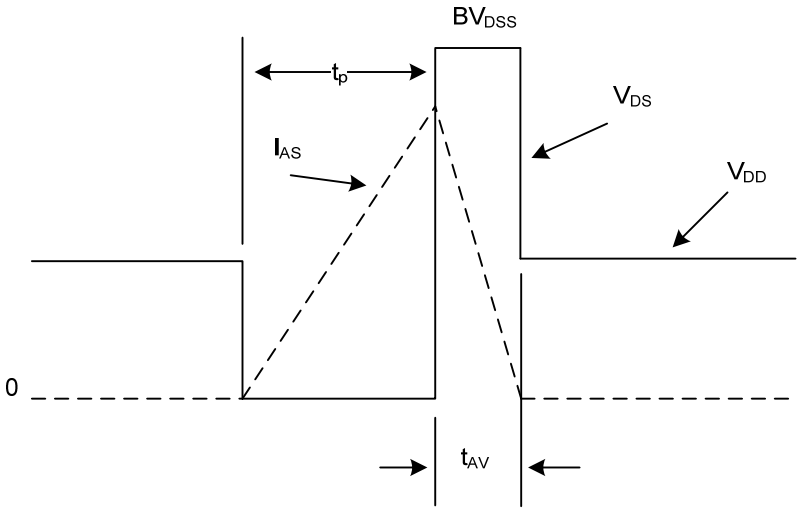


FIG 2. Unclamped Energy Waveforms

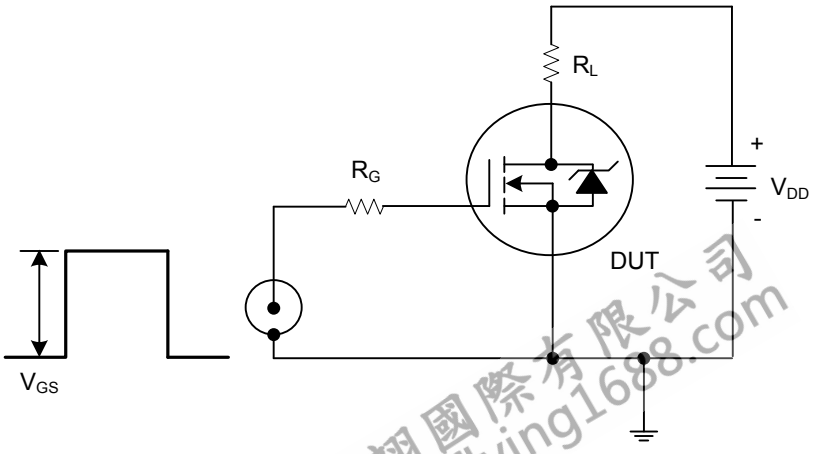


FIG 3. Switching Time Test Circuit

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

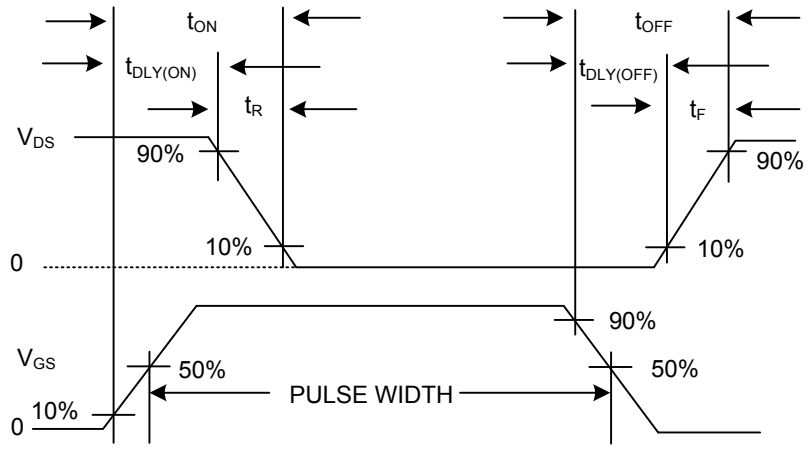


FIG 4. Resistive Switching Waveforms

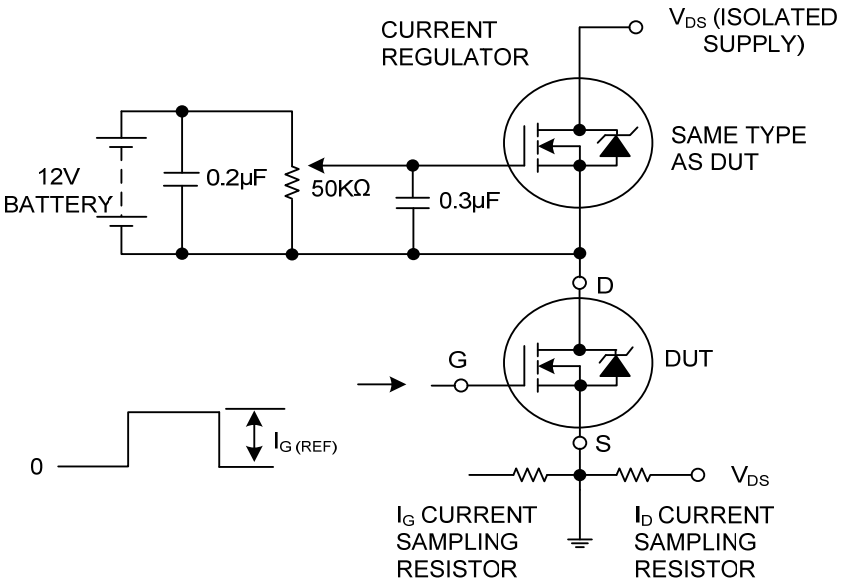


FIG 5. Gate Charge Test Circuit

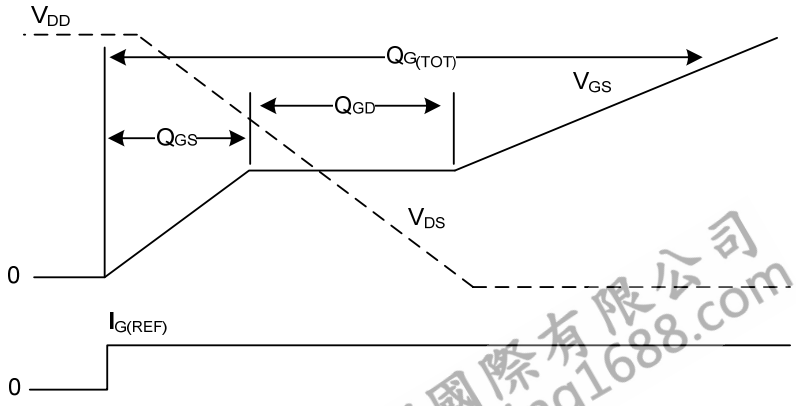
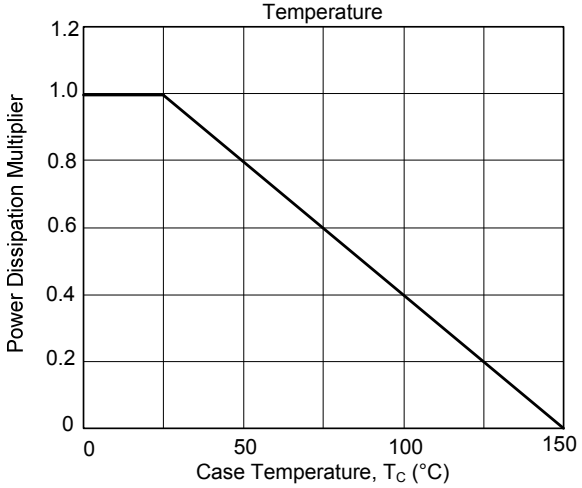


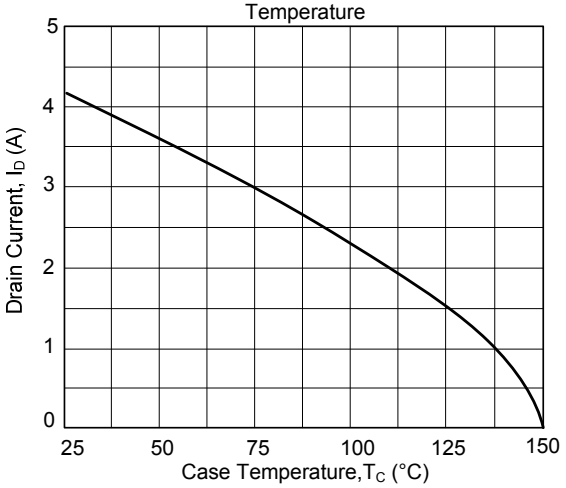
FIG 6. Gate Charge Waveforms

■ TYPICAL CHARACTERISTICS

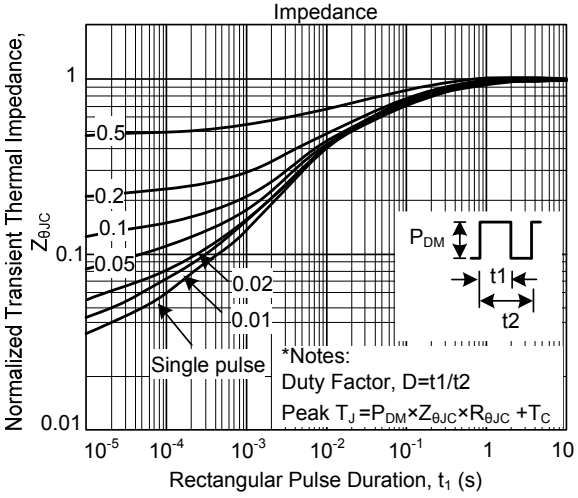
Normalized Power Dissipation vs. Case Temperature



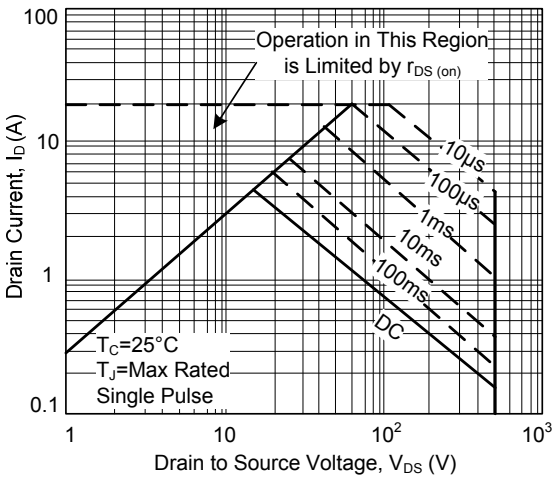
Maximum Contionuous Drain Current vs. Case Temperature



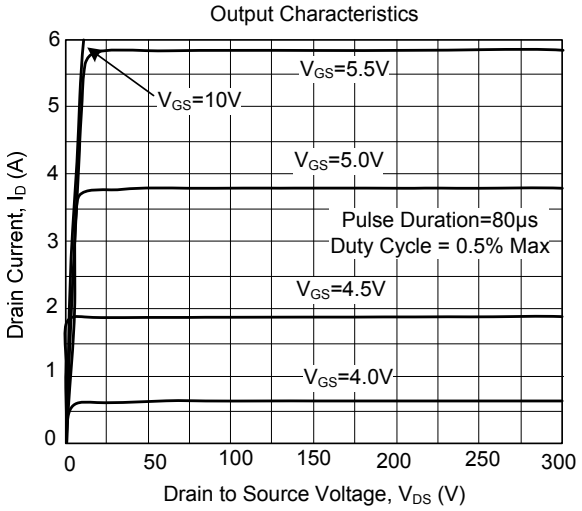
Normalized Maximum Transient Thermal Impedance



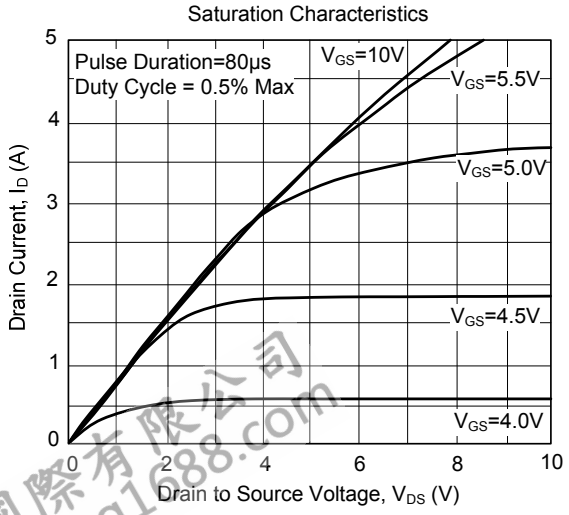
Forward Bias Safe Operating Area



Output Characteristics

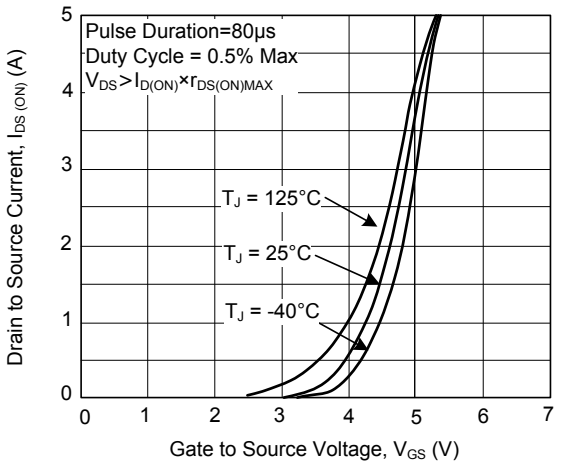


Saturation Characteristics

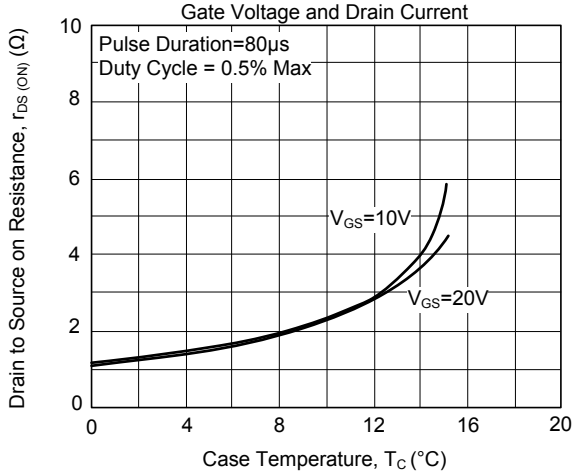


■ TYPICAL CHARACTERISTICS (Cont.)

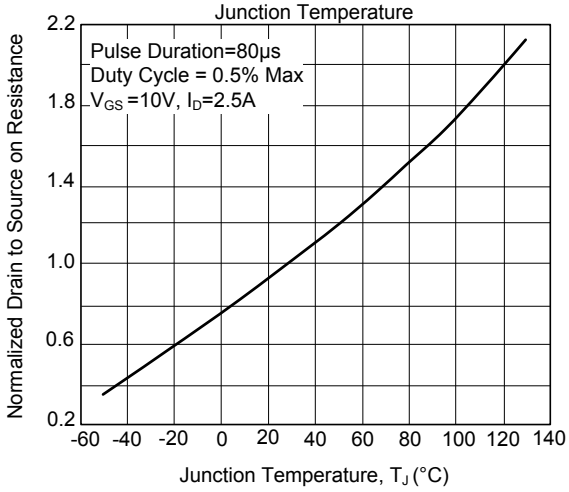
Transfer Characteristics



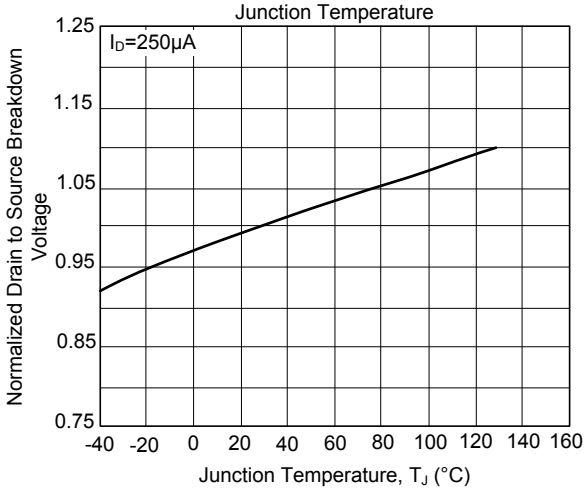
Drain to Source on Resistance vs. Gate Voltage and Drain Current



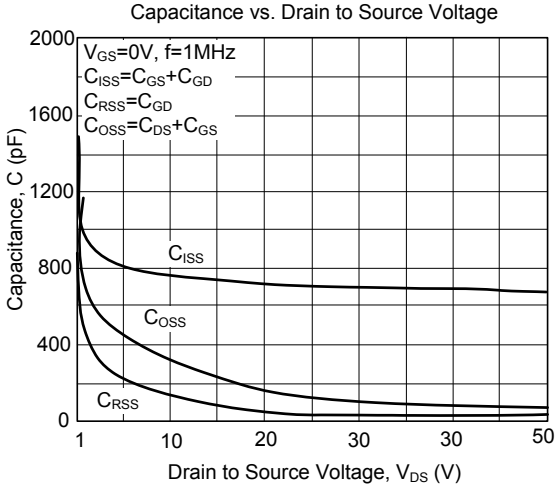
Normalized Drain to Source on Resistance vs. Junction Temperature



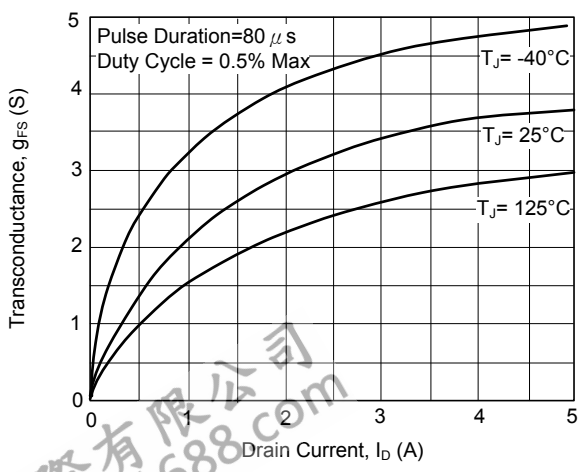
Normalized Drain to Source Breakdown Voltage vs. Junction Temperature



Capacitance vs. Drain to Source Voltage



Transconductance vs. Drain Current



■ TYPICAL CHARACTERISTICS (Cont.)