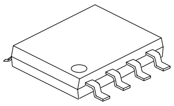
5.5MHZ, LOW VOLTAGE RAIL-TO-RAIL I/O CMOS DUAL OP AMPS



SOP-8

■ DESCRIPTION

The UTC **ULV8622** is low noise, low voltage and low power dual operational amplifiers that can be designed into a wide range of applications. With a 5.5MHz unity-gain frequency and a guaranteed 3.7V/μs slew rate, the quiescent current is only 480μA/amplifier (5.0V).

The UTC **ULV8622** provides rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground and the maximum input offset voltage is 3mV. It is specified over the extended industrial temperature range (-40°C~+125°C). The operating range is 2.0V~5.5V. The UTC **ULV8622** provides optimal performance in low voltage and low noise systems.

■ FEATURES

* Rail-to-Rail Input and Output
* Input Rail: -0.1V~+5.6V with V_S=5.5V
* Gain-Bandwidth Product: 5.5MHz
* High Slew Rate: 3.7V/μs
* Operates on 2.0V~5.5V Supplies
* Low Power: 480μA/Amplifier Typical Supply Current

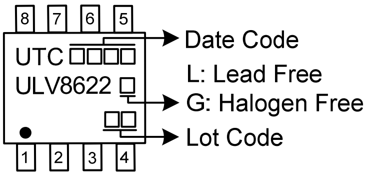
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULV8622L-S08-R	ULV8622G-S08-R	SOP-8	Tape Reel

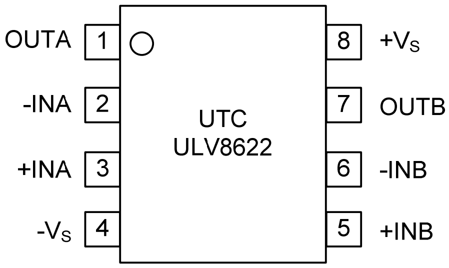
ULV8622G-S08-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) S08: SOP-8
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



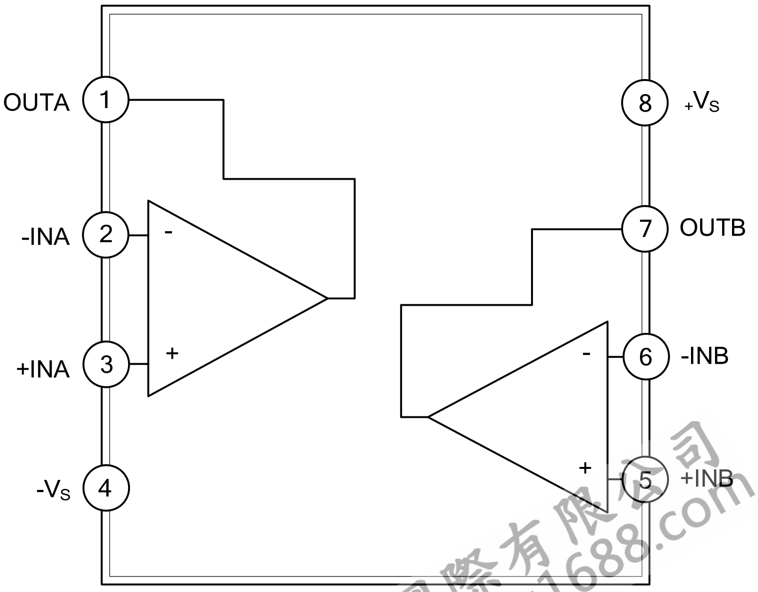
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	OUTA	Output of op amp A
2	-INA	Negative Input of op amp A
3	+INA	Positive Input of op amp A
4	-V_S	Negative Power Supply
5	+INB	Positive Input of op amp B
6	-INB	Negative Input of op amp B
7	OUTB	Output of op amp B
8	+V_S	Positive Power Supply

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=+25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage, V+ ~ V-	V_S	6	V
Common-Mode Input Voltage	V_{CM}	(-Vs)-0.3 ~ (+Vs)+0.3	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient @ T_A=25°C	θ_{JA}	125	°C/W

■ ELECTRICAL CHARACTERISTICS(T_A=+25°C,V_S=5V,V_{CM}=V_S/2,R_L=600Ω, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.9	3	mV
Input Bias Current	I_B			1		pA
Input Offset Current	I_{OS}			1		pA
Common-Mode Voltage Range	V_{CM}	V_S=5.5V		-0.1~+5.6		V
Common-Mode Rejection Ratio	CMRR	V_S=5.5V, V_{CM}=-0.1V~4V	65	84		dB
		V_S=5.5V, V_{CM}=-0.1V~5.6V		76		dB
Open-Loop Voltage Gain	A_{OL}	R_L=600Ω, Vo=0.15V~4.85V	75	92		dB
		R_L=10KΩ, Vo=0.05V~4.95V		103		dB
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta_T$			2.7		μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing from Rail	V_O	R_L=600Ω		0.1		V
		R_L=10KΩ		0.01		
Output Current	I_{OUT}		39	51		mA
Closed-Loop Output Impedance	R_O	F=200KHz, G=1		5.4		Ω
POWER SUPPLY						
Operating Voltage Range	V_S		2.0		5.5	V
Power Supply Rejection Ratio	PSRR	V_S=+2.5V~+5.5V,V_{CM}=(-V_S)+0.5V	70	84		dB
Quiescent Current/ Amplifier	I_Q	I_{OUT}=0		480	620	μA
DYNAMIC PERFORMANCE						
Gain-Bandwidth Product	G_{BP}	R_L=10KΩ		5.5		MHz
Phase Margin	φ_O			63		degrees
Full Power Bandwidth	BW_P	<1% Distortion		250		KHz
Slew Rate	SR	G=+1, 2V Output Step		3.7		V/μs
Settling Time To 0.1%	t_S	G=+1, 2V Output Step		2.1		μs
Overload Recovery Time	t_{OR}	V_{IN} · Gain=Vs		1		μs
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f=1kHz		13		$nV/\sqrt{Hz}$

■ APPLICATION NOTES

Driving a Capacitive Load

The UTC **ULV8622** can directly drive 1000pF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. It is recommended that an isolation resistor (R_{ISO}) is placed in series with the output of the amplifier when the greater capacitive load is required. The circuit is shown in Figure 1. The R_{ISO} and the load capacitor C_L form a zero to increase stability, but this method results in a loss of gain accuracy for R_{ISO} dividing the voltage with R_{LOAD}.

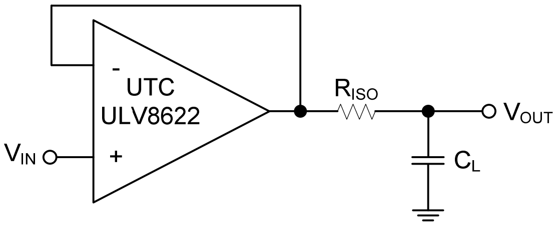


Figure 1. Indirectly Driving Heavy Capacitive Load

The circuit in Figure 2 provides DC accuracy and AC stability. To increase the DC accuracy, R_F should be connected between the inverting input and the output. To preserve the phase margin in the overall feedback loop, C_F is required and can compensate the loss of phase margin together with R_{Iso} by feeding the high frequency component of the output signal back to the amplifier's inverting input

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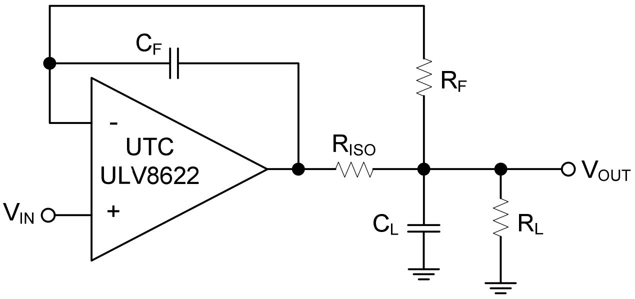

Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's closed-loop gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

■ APPLICATION NOTES(Cont.)

Power-Supply Bypassing and Layout

The UTC **ULV8622** can apply for a single +2V~+5.5V supply or dual ±1V~±2.75V supplies. For single-supply operation, a 0.1μF ceramic capacitor should be placed close to the V_{DD} pin to bypass the power supply V_{DD}. For dual-supply operation, separate 0.1μF ceramic capacitors should be placed to the V_{DD} and the V_{SS} supplies to bypass them to ground, and 2.2μF tantalum capacitor for better performance.

By decreasing the amount of stray capacitance at the op amp's inputs and output, PC board l performance can be optimized. For example, placing external components as close to the device as possible can minimize trace lengths and widths. and using surface-mount components is a better way.

For the operational amplifier, soldering the part to the board directly is strongly recommended. The EMI can be minimized because keeping the high frequency big current loop area small.

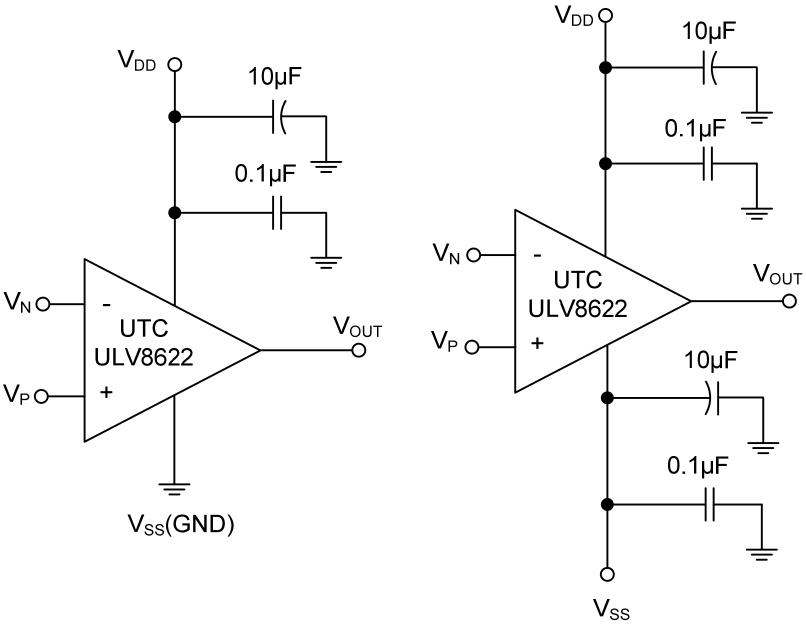

Figure 3. Amplifier with Bypass Capacitors

Grounding

A ground plane layer is important for UTC **ULV8622** circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

The input and output signal traces should not be parallel to minimize capacitive coupling. This helps reducing unwanted positive feedback.

■ TYPICAL APPLICATION CIRCUITS

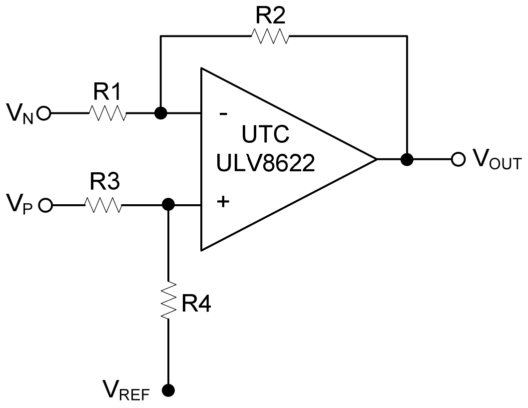

Figure 4. Differential Amplifier

Note: Figure 4 is the differential amplifier. If the resistors ratios are equal (R4/R3=R2/R1), then V_{OUT}=(Vp-Vn)×R2/R1+Vref.

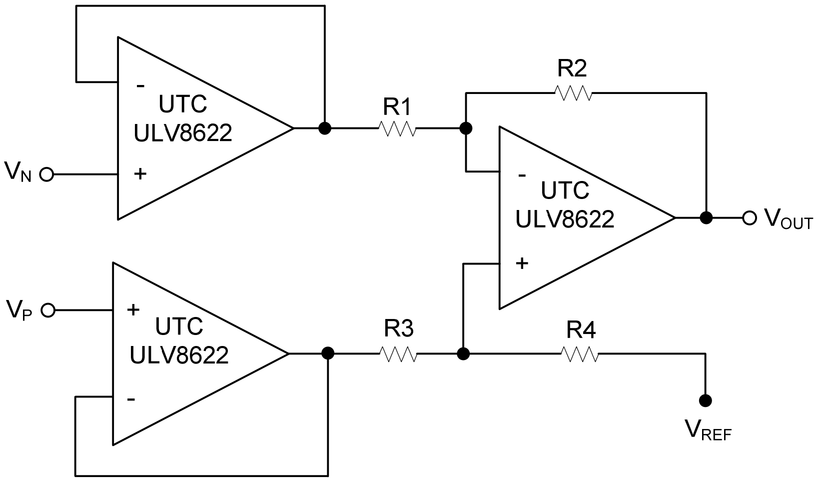

Figure 5. Instrumentation Amplifier

Note: Figure 5 performs the same function as that in Figure 4 but with the high input impedance.

- TYPICAL APPLICATION CIRCUITS (Cont.)

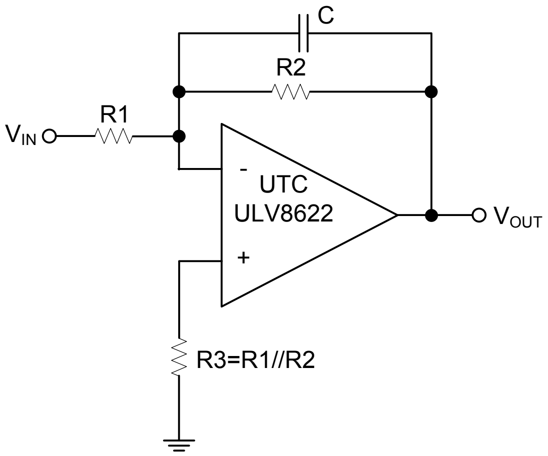

Figure 6. Low Pass Active Filter

Figure 6 is the low pass filter. It's DC gain is -R2/R1 and the -3dB corner frequency is 1/2πR$_2$C.