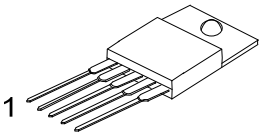
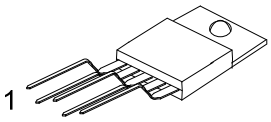
UMC33167

LINEAR INTEGRATED CIRCUIT

5.0A, STEP-UP/DOWN/ INVERTING SWITCHING REGULATORS



TO-220-5



TO-220B

■ DESCRIPTION

The UTC **UMC33167** series are high performance fixed frequency power switching regulators that contain the primary functions required for dc-to-dc converters. This series was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36μA.

■ FEATURES

* Output Switch Current in Excess of 5.0A
* Fixed Frequency Oscillator (72kHz) with On-Chip Timing
* Provides 5.05V Output without External Resistor Divider
* Precision 2% Reference
* 0% ~ 95% Output Duty Cycle
* Cycle-by-Cycle Current Limiting
* Undervoltage Lockout with Hysteresis
* Internal Thermal Shutdown
* Operation from 7.5V ~ 40V
* Standby Mode Reduces Power Supply Current to 36μA

■ ORDERING INFORMATION

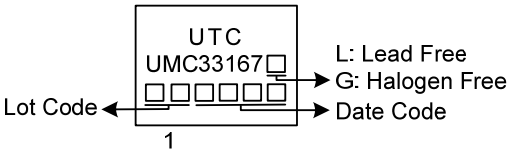
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UMC33167L-TA5-T	UMC33167G-TA5-T	TO-220-5	Tube
UMC33167L-TB5-T	UMC33167G-TB5-T	TO-220B	Tube

UMC33167G-TA5-T

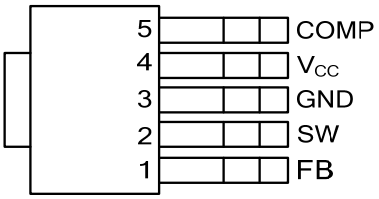
(1) Packing Type
(2) Package Type
(3) Green Package

(1) T: Tube
(2) TA5: TO-220-5, TB5: TO-220B
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	FUNCTION
1	FB	Output voltage feedback control
2	SW	Switch Output
3	GND	Gnd pin
4	V_{CC}	IC power supply pin
5	COMP	Compensation pin

■ BLOCK DIAGRAM

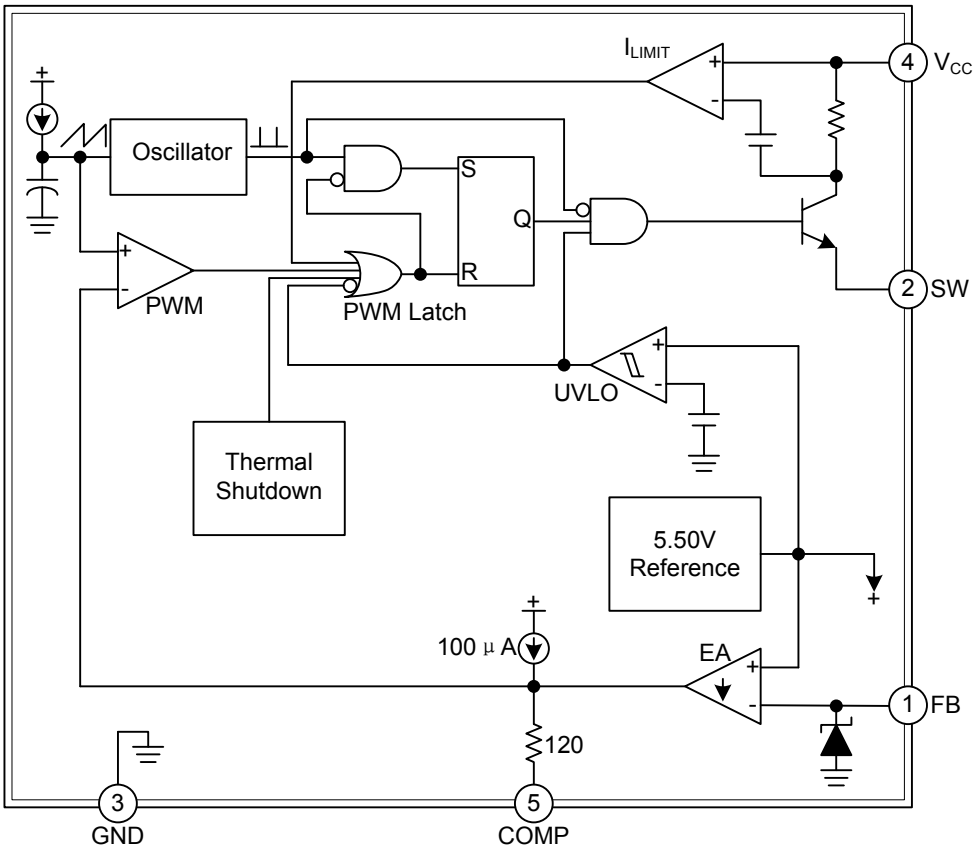


Figure 1 Simplified Block Diagram (Step Down Application)

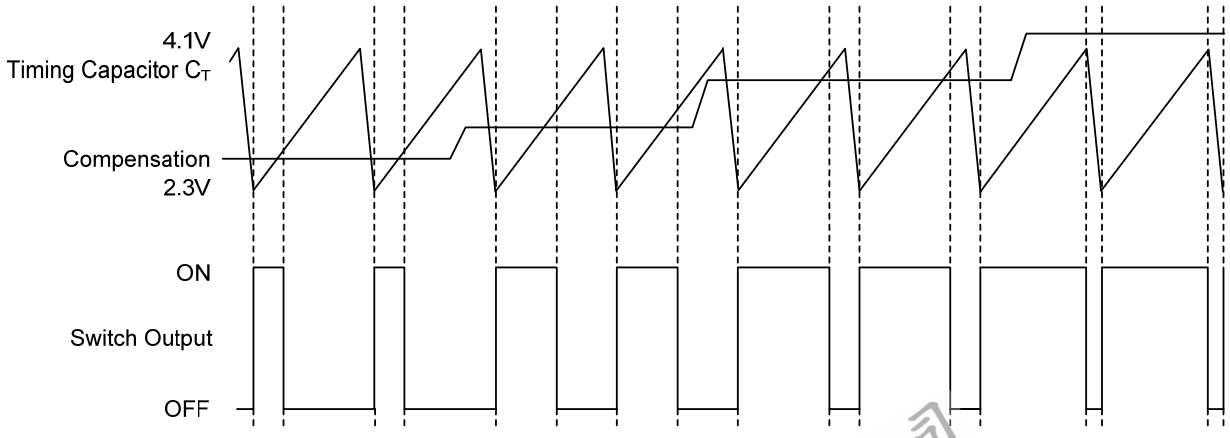


Figure 2. Timing Diagram

■ ABSOLUTE MAXIMUM RATING (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	-2.0 ~ +V_{IN}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB},V_{COMP}	-1.0 ~ +7.0	V
Power Dissipation (T_A=+25°C)	P_D	Internally Limited	W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
3. This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000V per MIL-STD-883, Method 3015.
Machine Model Method 200V.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	65	°C/W
Junction to Case	θ_{JC}	5.0	°C/W

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=12V, for typical values T_A=+25°C, for min/max values T_A is the operating ambient temperature range that applies (Notes 4), unless otherwise noted.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR							
Frequency (V_{CC}=7.5V ~ 40V)		f_{OSC}	T_A=+25°C	65	72	79	KH_Z
			T_J=T_{LOW} ~T_{HIGH}	62		81	KH_Z
ERROR AMPLIFIER							
Voltage Feedback Input Threshold		$V_{FB(th)}$	T_A=+25°C	4.95	5.05	5.15	V
			T_J=T_{LOW} ~T_{HIGH}	4.85		5.20	V
Line Regulation		Reg_{LINE}	V_{CC}=7.5V~ 40V, T_A=+25°C		0.03	0.078	%/V
Input Bias Current		I_{IB}	V_{FB}=$V_{FB(th)}$+0.15V		0.15	1.0	μA
Power Supply Rejection Ratio		PSRR	V_{CC}=7.5V~ 40V, f=120H_Z	60	80		dB
Output Voltage Swing	High State	V_{OH}	I_{SOURCE}=75μA, V_{FB}=4.5V	4.2	4.9		V
	Low State	V_{OL}	I_{SINK}=0.4mA, V_{FB}=5.5V		1.6	1.9	V
PWM COMPARATOR							
Duty Cycle (V_{CC}=20V)		$DC_{(max)}$	Maximum (V_{FB}=0V)	92	95	100	%
		$DC_{(min)}$	Minimum (V_{FB}=0V)	0	0	0	%
SWITCH OUTPUT							
Output Voltage Source Saturation		V_{SAT}	V_{CC}=7.5V, I_{SOURCE}=5.0A		V_{CC}-1.5	V_{CC}-1.8	V
Off-State Leakage		$I_{SW(off)}$	V_{CC}=40V, Pin 2 = GND		0	100	A
Current Limit Threshold		$I_{PK(switch)}$	V_{CC}=7.5V	5.5	6.5	8.0	A
Switching Times	Output Voltage Rise Time	t_R	V_{CC}=40V,I_{PK}=5.0A, L=225μH, T_A=+25°C		100	200	ns
	Output Voltage Fall Time	t_F			50	100	ns
UNDERVOLTAGE LOCKOUT							
Startup Threshold		$V_{th(UVLO)}$	V_{CC} Increasing, T_A=+25°C	5.5	5.9	6.3	V
Hysteresis		$V_{H(UVLO)}$	(V_{CC} Decreasing, T_A=+25°C	0.6	0.9	1.2	V
TOTAL DEVICE							
Power Supply Current (T_A=+25°C)	Standby	I_{CC}	V_{CC}=12V, V_{Comp}<0.15V		36	100	μA
	Operating		V_{CC}=40V, Pin 1=GND for maximum duty cycle		40	60	mA

Note 4: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

■ TYPICAL APPLICATION CURRENT

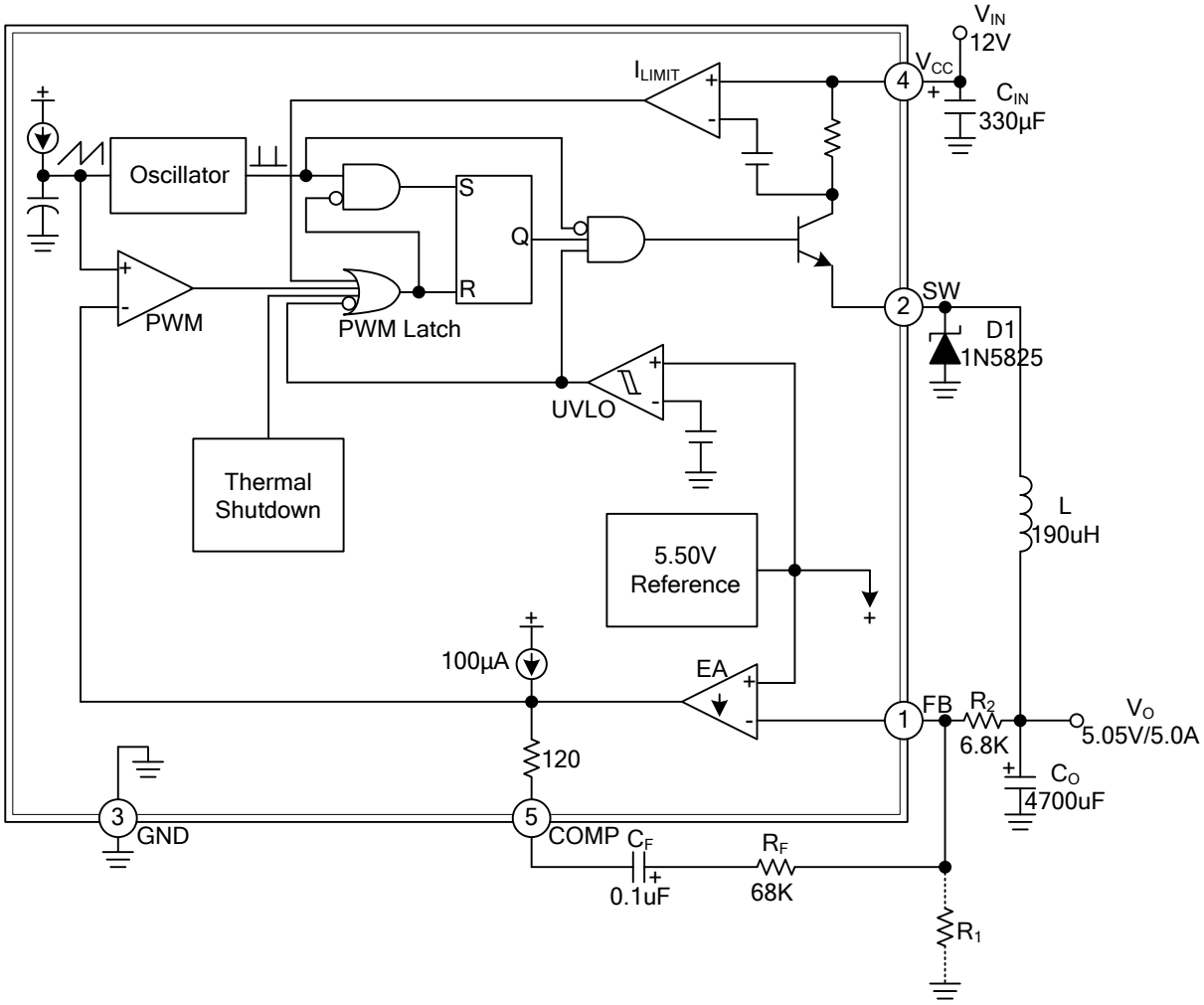


Figure 3. Step-Down Converter

The Step-Down Converter application is shown in Figure 3. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{IN} and V_{REF} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05V, resistor R_1 must be added to form a divider network at the feedback input.

■ APPLICATION INFORMATION

The UTC **UMC33167** series are monolithic power switching regulators that are optimized for dc-to-dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. They can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 1.

Oscillator

The oscillator frequency is internally programmed to 72kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1V and 2.3V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 2 illustrate the switch output duty cycle versus the compensation voltage.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80dB, and a unity gain bandwidth of 600kHz with 70 degrees of phase margin. The noninverting input is biased to the internal 5.05V reference and is not pinned out. The reference has an accuracy of ±2.0% at room temperature. To provide 5.0V at the load, the reference is programmed 50mV above 5.0V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05V, resistor R1 must be added to form a divider network at the feedback input as shown in Figures 1 and 3. The equation for determining the output voltage with the divider network is: $V_{OUT}=5.05(R_2/R_1+1)$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor-capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 3) is the easiest to compensate for stability. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting RF and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36A with a 12V supply voltage.

The Error Amplifier output has a 100 A current source pull-up that can be used to implement soft-start.

Switch Output

The output transistor is designed to switch a maximum of 40V, with a minimum peak collector current of 5.5A. When configured for step-down or voltage-inverting applications, as in Figures 3, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. shows that by clamping the emitter to 0.5V, the collector current will be in the range of 100A over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

■ APPLICATION INFORMATION (Cont.)

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9V. To prevent erratic output switching as the threshold is crossed, 0.9V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking. The UTC **MC34167** is contained in a 5-lead TO-220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.