



UNA15R185H

POWER MOSFET

83A, 150V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

DESCRIPTION

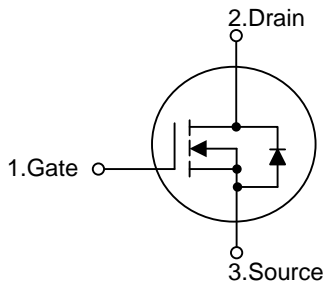
The UTC **UNA15R185H** is N-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with ideal for low voltage inverter applications.

The UTC **UNA15R185H** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

- * $R_{DS(ON)} \leq 18.5 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=40\text{A}$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL

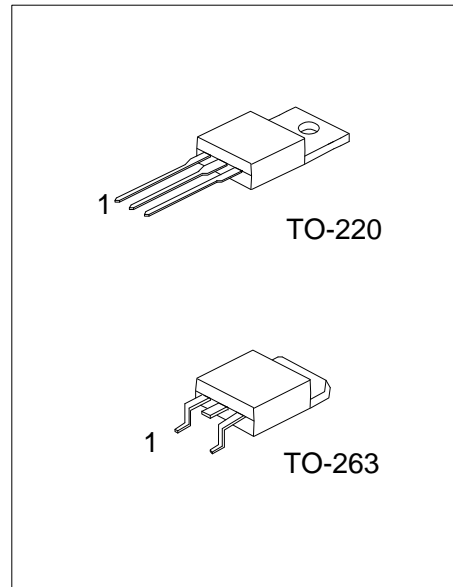


ORDERING INFORMATION

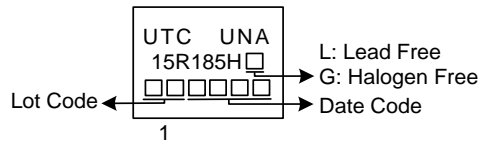
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UNA15R185HL-TA3-T	UNA15R185HG-TA3-T	TO-220	G	D	S	Tube
UNA15R185HL-TQ2-T	UNA15R185HG-TQ2-T	TO-263	G	D	S	Tube
UNA15R185HL-TQ2-R	UNA15R185HG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UNA15R185HG-TA3-T	(1)Packing Type	(1) T: Tube, R: Tape Reel
	(2)Package Type	(2) TA3: TO-220, TQ2: TO-263
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



MARKING



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■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	150	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current	Continuous	I _D	83	A
Pulsed Drain Current	Pulsed (Note 2)	I _{DM}	249	A
Avalanche Current (Note 3)		I _{AR}	63	A
Avalanche energy	Single Pulsed (Note 3)	E _{AS}	198	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	8.9	V/nS
Power Dissipation		P _D	190	W
Junction Temperature		T _J	+150	°C
Storage Temperature Range		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L=0.1mH, I_{AS}=63A, V_{DD}=50V, R_G=25Ω, Starting T_J = 25°C.

4. I_{SD} ≤ 30A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J = 25°C.

■ THERMAL DATA

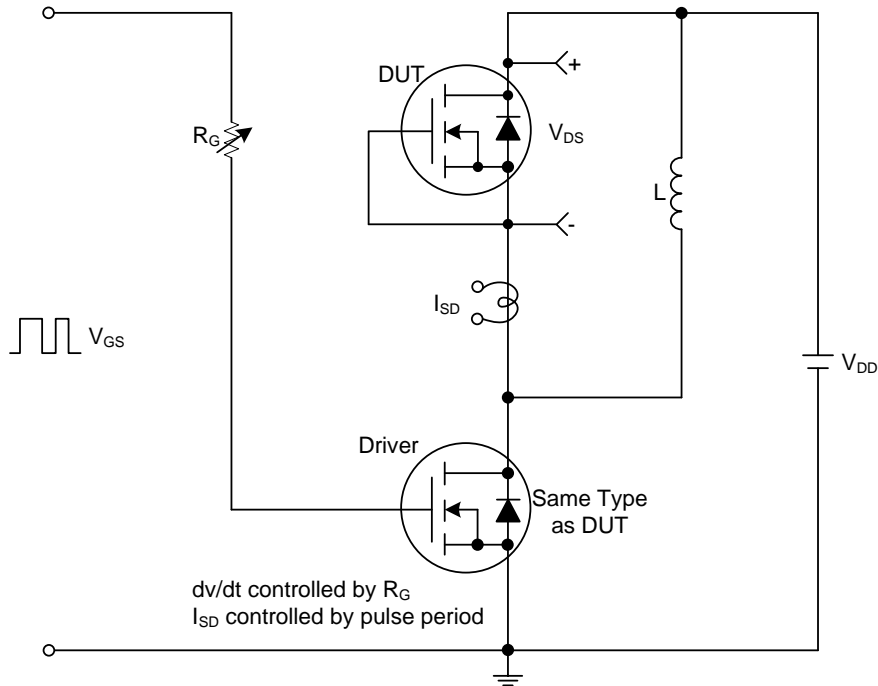
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ _{JA}	62.5	°C/W
Junction to Case	θ _{JC}	0.66	°C/W

■ **ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$, unless otherwise specified)

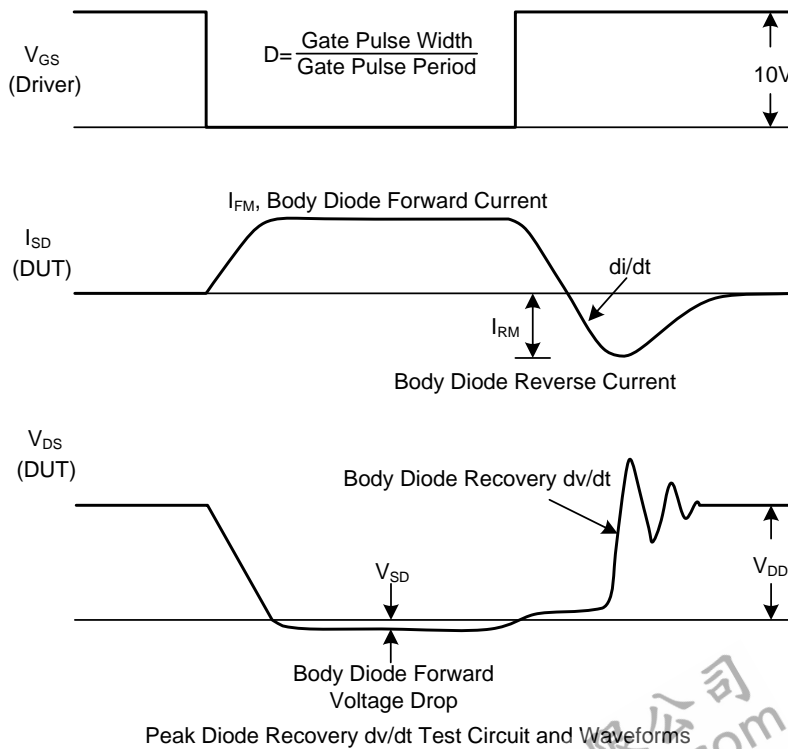
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	150			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=150\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=40\text{A}$		14.5	18.5	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$		6930		pF
Output Capacitance	C_{OSS}			550		pF
Reverse Transfer Capacitance	C_{RSS}			200		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$, $I_D=100\mu\text{A}$ (Note 1, 2)		450		nC
Gate to Source Charge	Q_{GS}			50		nC
Gate to Drain Charge	Q_{GD}			38		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		240		ns
Rise Time	t_R			180		ns
Turn-off Delay Time	$t_{D(OFF)}$			1040		ns
Fall-Time	t_F			300		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				83	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				249	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=40\text{A}$, $V_{GS}=0\text{V}$			1.2	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S=30\text{A}$, $V_{GS}=0\text{V}$, $di/dt=100\text{A}/\mu\text{S}$		84		nS
Reverse Recovery Charge	Q_{rr}			260		nC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature.

TEST CIRCUITS AND WAVEFORMS



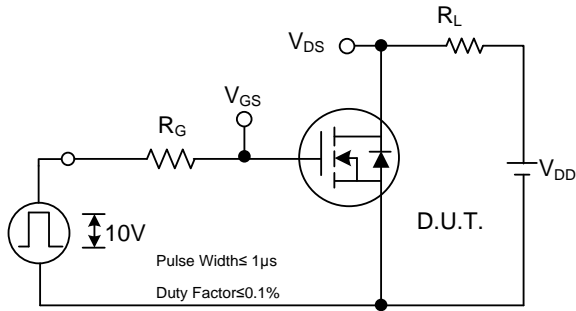
Peak Diode Recovery dv/dt Test Circuit



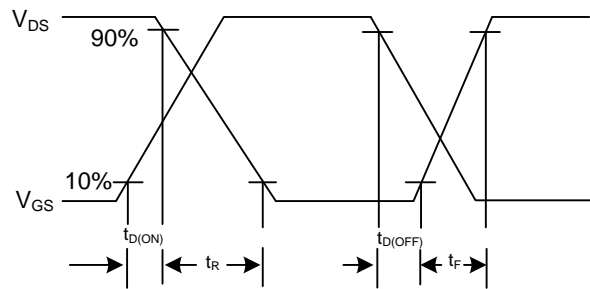
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

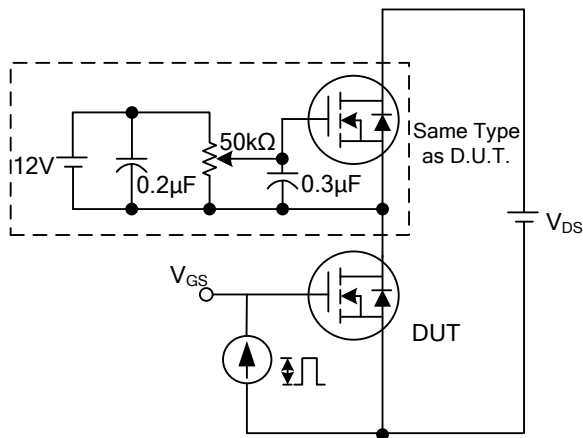
TEST CIRCUITS AND WAVEFORMS



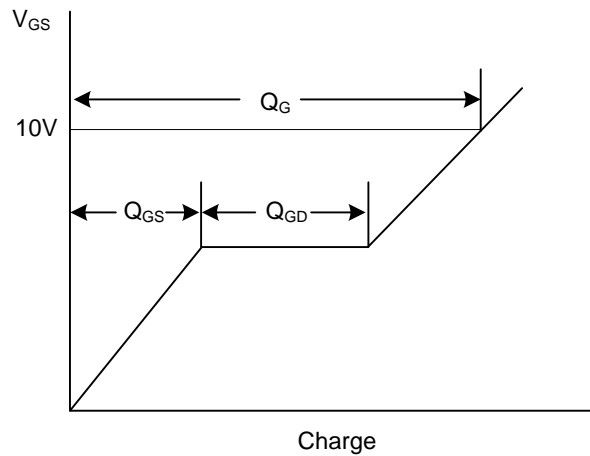
Switching Test Circuit



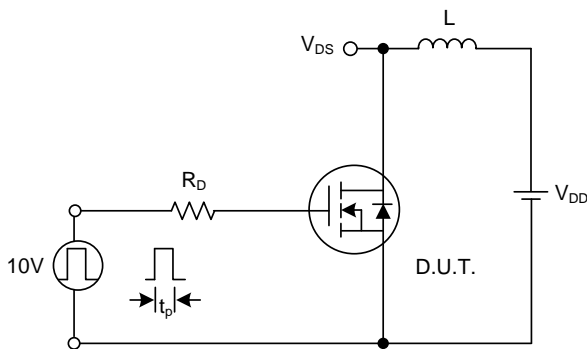
Switching Waveforms



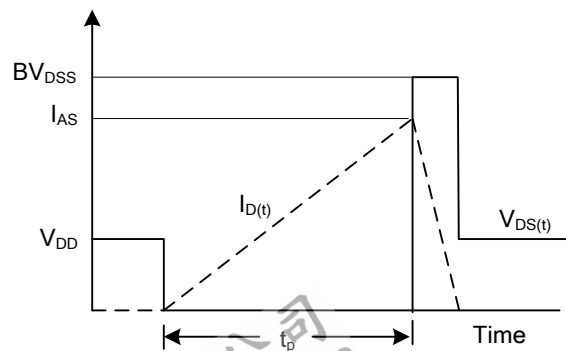
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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