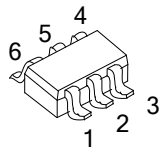
HIGH PRECISION CC/CV PRIMARY-SIDE PWM CONTROLLER



SOT-26

■ DESCRIPTION

The UTC **UPSR104** is a primary controller mode charger and adapter applications. The controlled variable is transferred by an auxiliary winding from the secondary to the primary side. The device integrates PWM controller to enhance the performance of discontinuous conduction mode (DCM) flyback converters.

The UTC **UPSR104** operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. It also provides off-time modulation to linearly decrease PWM frequency under light-load conditions so that low standby power can be achieved.

The UTC **UPSR104** achieves high precision CV/CC regulation and high power efficiency. It offers comprehensive protection coverage with auto-recovery features including Cycle-by-cycle current limiting, VDD over voltage protection, VDD clamp, OTP, leading edge blanking, VDD under voltage lockout, etc.

■ FEATURES

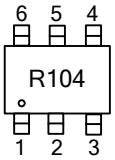
* ±5% Constant Voltage Regulation at Universal AC input
* High Precision Constant Current Regulation at Universal AC input
* Primary-side Sensing and Regulation Without TL431 and Opto-coupler
* Programmable CV and CC Regulation
* Adjustable Constant Current and Output Power Setting
* Built-in Secondary Constant Current Control with Primary Side Feedback
* Built-in Adaptive Current Peak Regulation
* Built-in Primary winding inductance compensation
* Programmable Cable drop Compensation
* Power on Soft-start
* Built-in Leading Edge Blanking (LEB)
* Cycle-by-Cycle Current Limiting
* V_{DD} Under Voltage Lockout with Hysteresis (UVLO)
* V_{DD} OVP
* V_{DD} Clamp

■ ORDERING INFORMATION

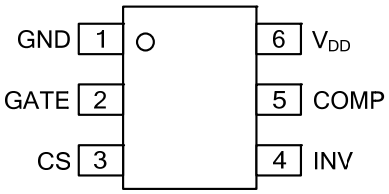
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UPSR104L-AG6-R	UPSR104G-AG6-R	SOT-26	Tape Reel

UPSR104G-AG6-R	
(1) Packing Type	(1) R: Tape Reel
(2) Package Type	(2) AG6: SOT-26
(3) Green Package	(3) G : Halogen Free and Lead Free, L: Lead Free

■ MARKING



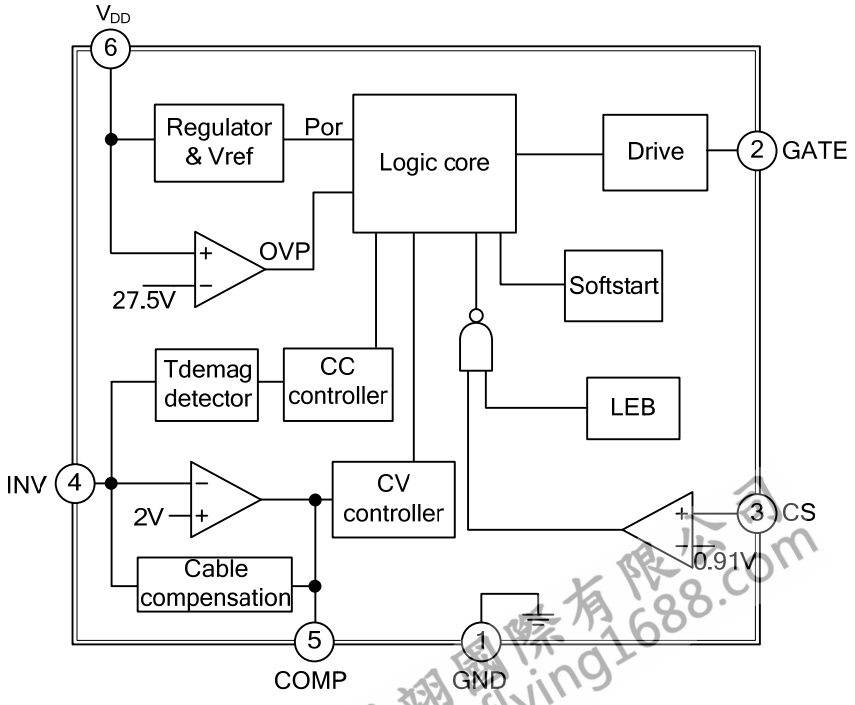
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground
2	GATE	Totem-pole gate drive output for power MOSFET.
3	CS	Current sense input. Connected to MOSFET current sensing resistor node.
4	INV	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
5	COMP	Loop Compensation for CV Stability
6	V_{DD}	Power Supply

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
V_{DD} Voltage	V_{DD}	-0.3 ~ $V_{DD\_}$ Clamp	V
V_{DD} Zener Clamp Continuous Current		10	mA
COMP Voltage	V_{COMP}	-0.3 ~ 7	V
CS Input Voltage	V_{CS}	-0.3 ~ 7	V
INV Input Voltage	V_{INV}	-0.3 ~ 7	V
Max Operating Junction Temperature	T_J	+150	°C
Min/Max Storage Temperature	T_{STG}	-55 ~ +150	°C
Lead Temperature (Soldering, 10secs)	T_{OPR}	+260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (TA=25°C, VDD=16V, if not otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (V_{DD}) Section						
Standby Current	I_{DD_ST}	V_{DD}=13V		2	5	uA
Operation Current	I_{DD_OP}	Operation supply current, INV=2V, CS=0V, VDD=18V		1.6	3	mA
V_{DD} Under Voltage Lockout Enter	UVLO_(ON)	V_{DD} falling	8.0	9.0	10.0	V
V_{DD} Under Voltage Lockout Exit	UVLO_(OFF)	V_{DD} rising	13.5	14.8	16.0	V
Maximum V_{DD} Operation Voltage	V_{DD_CLAMP}	I_{DD}=10mA		29		V
Over Voltage Protection Threshold	OVP	Ramp V_{DD} until gate shut down	26	27.5	29	V
Current Sense Input Section						
LEB Time	TLEB			600		ns
Over Current Threshold	V_{TH_OC}		880	910	940	mV
OCP Propagation delay	T_{d_OC}			60		ns
Soft Start Time	$T_{\_SS}$			17		ms
Frequency Section						
IC Maximum Frequency	F_{req_Max}	(Note 1)	60	65	70	KHz
System Nominal Switch Frequency	F_{req_Nom}			55		KHz
	$F_{req\_startup}$	INV=0V, Comp=5V		14		KHz
Δf/Freq	Frequency shuffling range			±6		%
Error Amplifier Section						
Reference Voltage for EA	V_{REF_EA}		1.97	2	2.03	V
DC Gain of EA	Gain			60		dB
Max. Cable Compensation Current	I_{COMP_MAX}	INV=2V, Comp=0V		37		uA
Gate Drive Output Section						
Output Low Level	V_{OL}	I_O=20mA			1	V
Output High Level	V_{OH}	I_O=20mA	8			V
Output Clamp Voltage Level	V_{clamp}			16		V
Output Rising Time	$T_{\_r}$	C_L=0.5nF		220		ns
Output Falling Time	$T_{\_f}$	C_L=0.5nF		40		ns
On chip OTP Section						
Over Temperature protection	OTP			150		℃

Note: F_{req_Max} indicates IC internal maximum clock frequency. In system application, the maximum operation frequency of 65Khz nominal occurs at maximum output power or the transition point from CV to CC.

■ OPERATION DESCRIPTION

The UTC **UPSR104** is a primary controller mode charger and adapter applications. It operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve high precision CV/CC performance. The device integrates PWM controller to enhance the performance of discontinuous conduction mode (DCM) flyback converters.

Startup Control

The V_{DD} pin of UTC **UPSR104** is connected to the line input through a resistor. A large value startup resistor can be used to minimize the power loss in application because the start current of UTC **UPSR104** is very low. When the VDD voltage reaches $V_{TH\ (ON)}$, the internal startup circuit is disabled and the IC turns on.

Operating Current

The Operating current of UTC **UPSR104** is as low as 1.6mA. Good efficiency and very low standby power can be achieved.

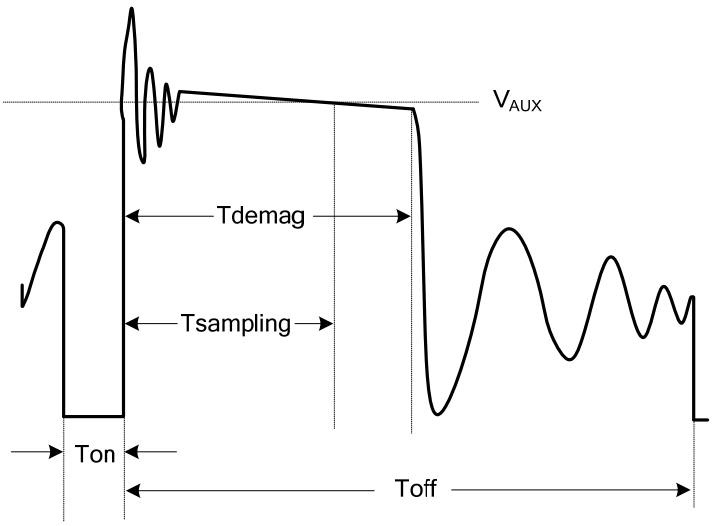
Constant Voltage Operation

The output voltage is defined by the transmission ratio between the secondary and auxiliary winding. The UTC **UPSR104** captures the auxiliary winding feedback voltage at INV pin and operates in constant-voltage (CV) mode to regulate the output voltage. The auxiliary voltage reflects the output voltage is given by:

$$V_{AUX} = \frac{N_A}{N_S} \times (V_O + \Delta V) \qquad (1)$$

Where ΔV indicates the drop voltage of the output diode.

Auxiliary Voltage Waveform



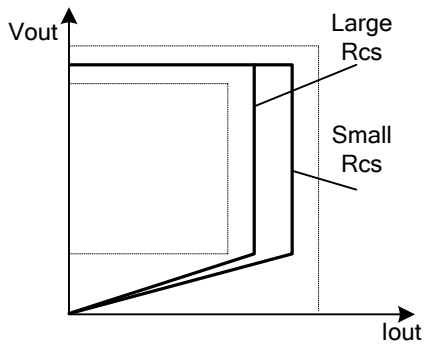
Via a resistor divider connected between the auxiliary winding and INV, the V_{AUX} is sampled at the Tsampling end and it is hold until the next sampling. The sampled voltage is compared with 2.0V reference voltage and the error is amplified. The error amplifier output reflects the load condition and controls the Toff time and the Ipk to regulate the output voltage, thus constant output voltage can be achieved.

Constant Current Operation

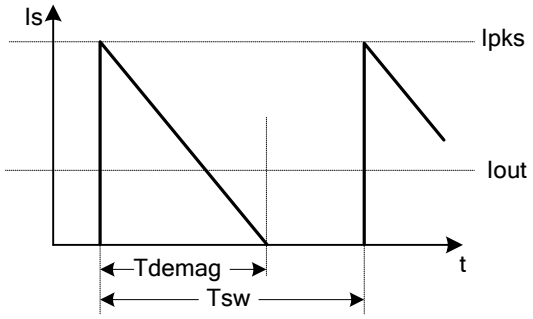
When the sampled voltage is below 2.0V reference voltage and the error amplifier output reaches its maximum, thus UTC **UPSR104** operates in constant-current (CC) mode. The CC point and maximum output power can be externally adjusted by external current sense resistor Rcs. The larger Rcs, the smaller CC point is, and the smaller output power becomes.

■ OPERATION DESCRIPTION (Cont.)

Adjustable Output Power By Changing Rcs



Secondary Current Waveform



In CC operation, the CC loop control function of UTC **UPSR104** will keep a fixed proportion between secondary inductance de-magnetization time (Tdemag) and switching cycle time (Tsw). The fixed proportion is

$$\frac{Tdemag}{Tsw} = \frac{1}{2} \qquad (2)$$

Thus the output current is given by:

$$Iout = \frac{1}{2} \times \frac{N_P}{N_S} \times Ipk \times \frac{Tdemag}{Tsw} = \frac{1}{4} \times \frac{N_P}{N_S} \times Ipk \qquad (3)$$

Programmable Cable Drop Compensation

UTC **UPSR104** has a built-in cable voltage drop compensation to achieve good load regulation. An offset voltage is generated at INV pin by an internal current flowing into the resistor divider. The current is inversely proportional to the voltage of COMP pin. As a result, it is inversely proportional to the output load current. The voltage drop across the cable is compensated by this offset voltage at INV pin. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used.

Current Sensing and Leading Edge Blanking

Cycle-by-cycle current limiting is offered in UTC **UPSR104**. The switch current is detected by a sense resistor into the CS pin. When the power switch is turned on, a turn-on spike will occur on this resistor. A 600ns leading-edge blanking is built in to avoid false-termination of the switching pulse so that the external RC filtering is no longer needed.

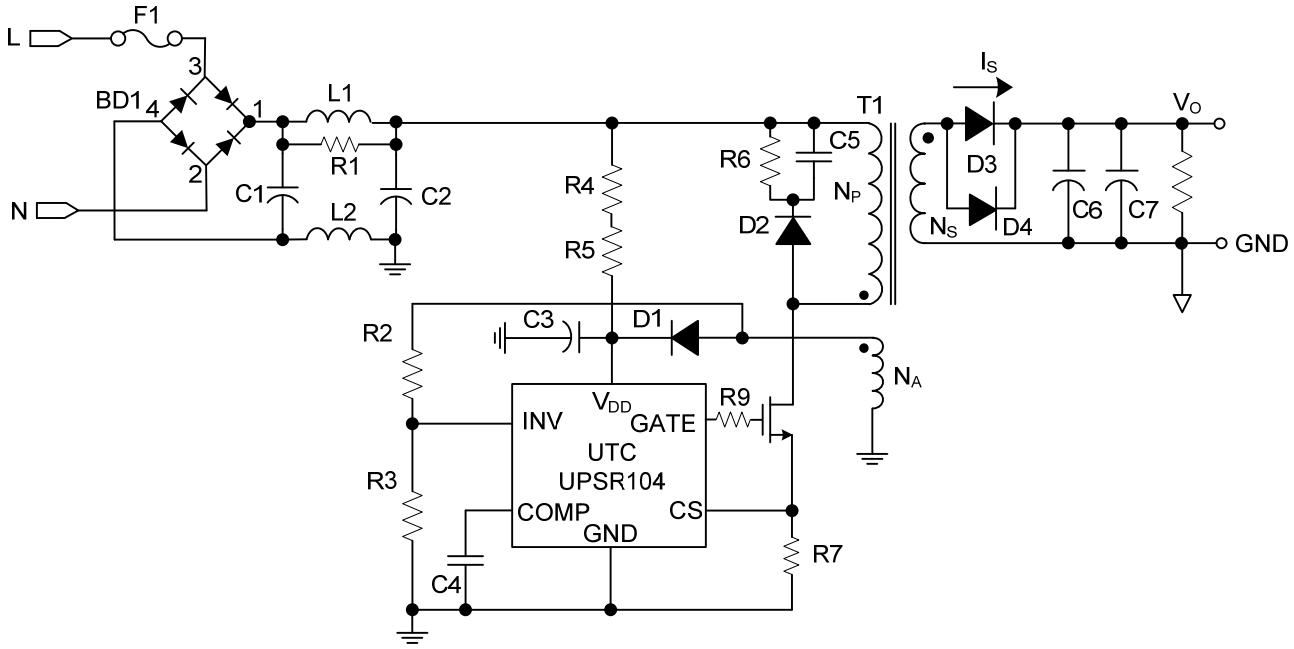
■ OPERATION DESCRIPTION (Cont.)

Protection Control

Good power supply system reliability is achieved with its comprehensive protection features including VDD over-voltage protection, VDD Clamp, GATE Clamp, Power on soft start, Cycle-by-cycle current limiting, short circuit protection, leading edge blanking, OTP and UVLO, etc.

VDD is supplied by transformer auxiliary winding output. The output of UTC **UPSR104** is shutdown when VDD drops below $V_{TH\ (OFF)}$ and the power converter enters power on start-up sequence thereafter.

■ TYPICAL APPLICATION CIRCUIT (12V / 1.25A)



BOM

Reference	Component	Reference	Component
BD1	BD 1.5A/600V	R1	R 2.4KΩ 1206 ±5%
L1	500u H DR 6x8mm	R2	R 33KΩ 0805 ±1%
L2	4.7u H 1W	R3	R 4.3KΩ 0805 ±1%
C1	EC 10u F 400V 105°C	R4	R 1.5MΩ 1206 ±5%
C2	EC 22u F 400V 105°C	R5	R 1.5MΩ 1206 ±5%
C3	EC 4.7u F 50V 105°C	R6	R 200KΩ 1206 ±5%
C4	CC 1n F 50V 0805	R7	R 0.9Ω 1206 ±5%
C5	CC 1n F 1000V 1206	R8	R 2.7KΩ 1206 ±5%
C6	EC 680u F 16V 105°C Low-ESR	R9	R 30Ω 0805 ±5%
C7	EC 680u F 16V 105°C Low-ESR	Q1	N-MOSFET UTC 2N60
D1	Diode UTC 1N4007G	T1	EF-20
D2	Diode UTC 1N4007G	F1	FUSE 2A 250VAC
D3	Diode UTC SB3100		
D4	Diode UTC SB3100		