



**UR6511**

Preliminary

**LINEAR INTEGRATED CIRCUIT**

**2A DDR BUS TERMINATION  
REGULATOR**

■ **DESCRIPTION**

The **UR6511** is a linear regulator providing up to 2A transient current sourcing and sinking capability for DDR bus terminator applications while regulating an output voltage to within 20mV. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

The **UR6511** output termination voltage tracks the reference voltage applied at  $V_{REF}$  pin. A resistor divider connected to  $V_{IN}$ , GND and  $V_{REF}$  pins is used to force the reference voltage to  $V_{REF}$  pin. Additional features include current limiting protection and thermal shutdown protection.

■ **FEATURES**

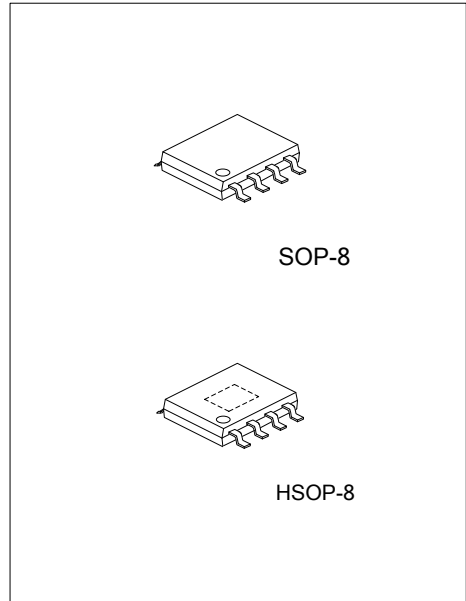
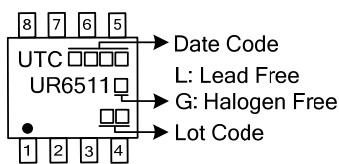
- \*DDR1/ DDR2/DDR3/Low Power DDR3 termination voltage applications
- \*Sink and Source Current: 2A
- \*Low output voltage offset within 20mV
- \*Adjustable output voltage by external resistors
- \*Integrated power MOS devices
- \*Suspend to RAM(STR) functionality
- \*Current Limiting Protection
- \*Thermal Shutdown Protection
- \*Cost-effective and easy to use

■ **ORDERING INFORMATION**

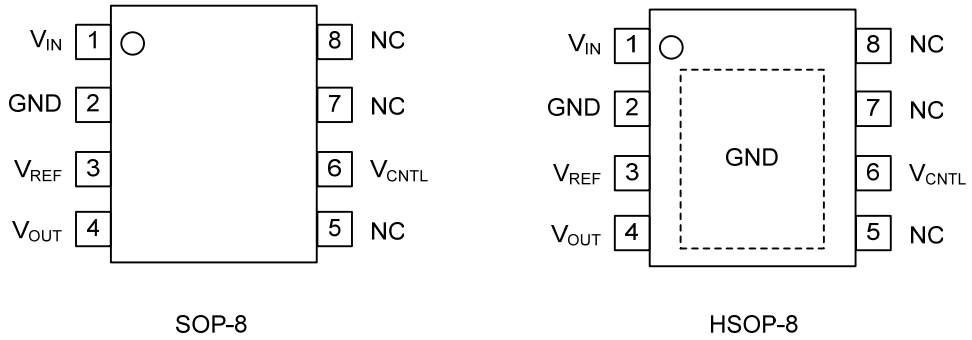
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UR6511L-S08-R	UR6511G-S08-R	SOP-8	Tape Reel
UR6511L-SH2-R	UR6511G-SH2-R	HSOP-8	Tape Reel

<p>UR6511G-S08-R</p>	<p>(1) R: Tape Reel (2) S08: SOP-8, SH2: HSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ **MARKING**



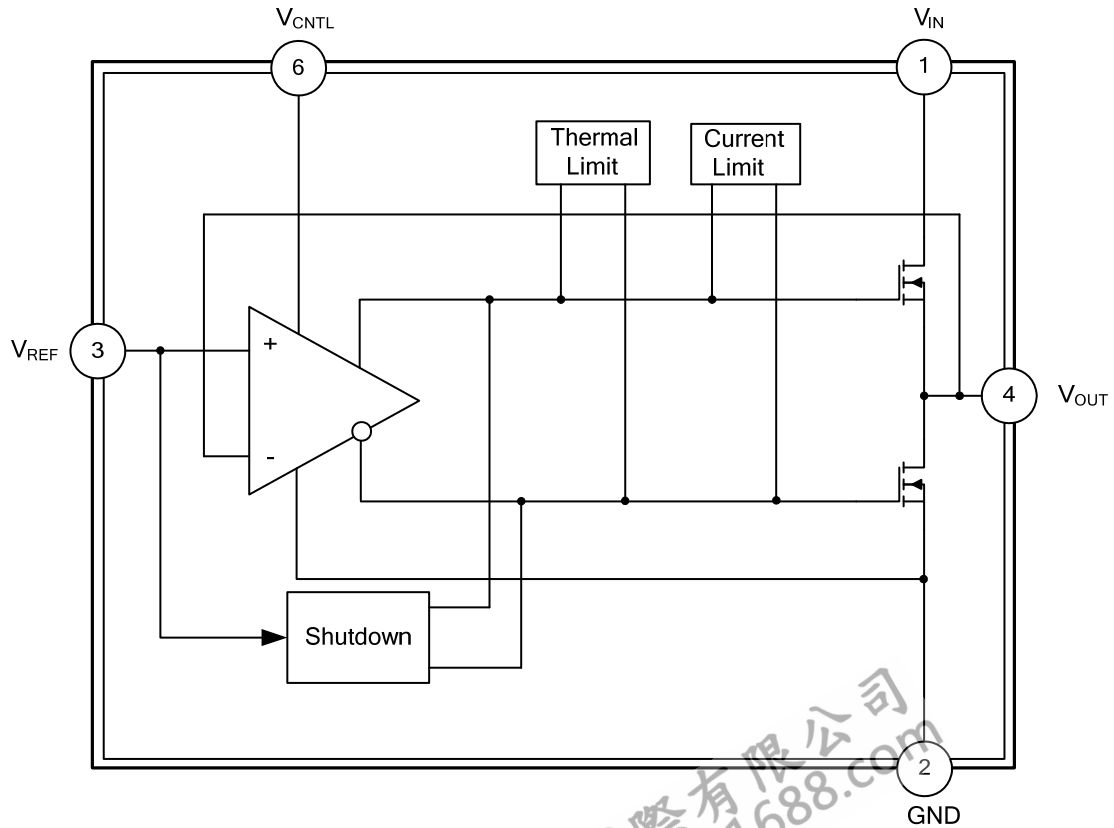
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

No.	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	V <sub>IN</sub>	I	Power supply pin for the V <sub>OUT</sub> output
2	GND	O	Ground pin
3	V <sub>REF</sub>	I	Reference voltage input and active-low shutdown control pin
4	V <sub>OUT</sub>	O	Output voltage pin
5, 7, 8	NC		
6	V <sub>CNTL</sub>	I	Power supply pin for the internal control circuits

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V <sub>CNTL</sub> Control Voltage	V <sub>CNTL</sub>	7	V
V <sub>IN</sub> Supply Voltage	V <sub>IN</sub>	7	V
Power Dissipation (T <sub>A</sub> =25°C)	P <sub>D</sub>	0.87	W
Junction Temperature	T <sub>J</sub>	+150	°C
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ <sub>JA</sub>	143	°C/W
Junction to Case	θ <sub>JC</sub>	45	°C/W

■ RECOMMENDED OPERATING CONDITIONS (Note)

PARAMETER	SYMBOL	RATINGS	UNIT
V <sub>CNTL</sub> Control Voltage	V <sub>CNTL</sub>	3.0 ~ 5.5	V
V <sub>IN</sub> Supply Voltage	V <sub>IN</sub>	1.0 ~ 5.5	V
Junction Temperature	T <sub>J</sub>	-40 ~ +125	°C
Ambient Temperature	T <sub>A</sub>	-40 ~ +85	°C

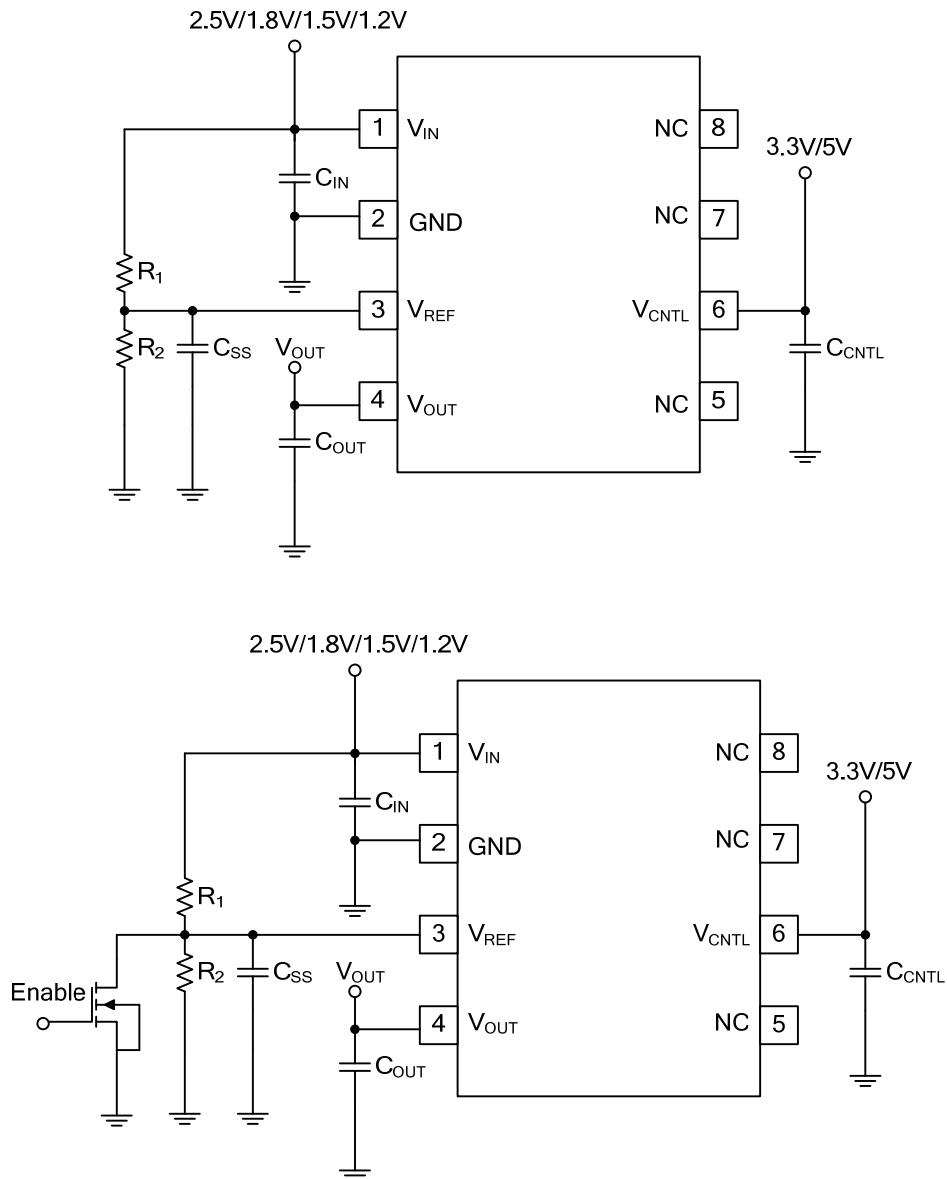
Note: All voltage values are with respect to the network ground terminal unless otherwise noted.

■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C, unless otherwise specified)

(V<sub>IN</sub>=2.5V/1.8V/1.5V, V<sub>CNTL</sub>=3.3V/5V, V<sub>REF</sub>=1.25V/0.9V/0.75V, C<sub>OUT</sub> = 10μF (Ceramic))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CURRENT</b>						
Operation Current of V <sub>CNTL</sub>	I <sub>CNTL</sub>	I <sub>OUT</sub> = 0A, V <sub>CNTL</sub> = 5V		0.7	1.5	mA
Standby Current	I <sub>STB</sub>	V <sub>REF</sub> < 0.15V, V <sub>CNTL</sub> = 5V		30	50	μA
<b>OUTPUT VOLTAGE (DDR/DDR II/DDR III)</b>						
Output Voltage Offset (V <sub>REF</sub> -V <sub>OUT</sub> )	V <sub>OS</sub>	I <sub>OUT</sub> = 0A	-10		10	mV
Load Regulation	ΔV <sub>LOAD</sub>	I <sub>OUT</sub> = ±2A	-20		20	mV
<b>PROTECTION</b>						
Current Limit	I <sub>LIMIT</sub>		2			A
Thermal Shutdown Temperature	T <sub>SD</sub>	V <sub>CNTL</sub> = 3.3V~5V		165		°C
Thermal Shutdown Hysteresis	ΔT <sub>SD</sub>	V <sub>CNTL</sub> = 3.3V~5V		30		°C
<b>V<sub>REF</sub> Shutdown</b>						
Shutdown Threshold	V <sub>IH</sub>	Enable	0.4			V
	V <sub>IL</sub>	Shutdown			0.15	V

■ TYPICAL APPLICATIONS CIRCUITS



$R_1=R_2=1\text{K}\Omega\sim 5\text{K}\Omega$ ,  $C_{OUT}=10\mu\text{F}$ (Ceramic)under the worst case testing condition

$C_{SS}=0.1\mu\text{F}$  to  $1\mu\text{F}$ ,  $C_{IN}=10\mu\text{F}$ (Low ESR),  $C_{CNTL}=0.1\mu\text{F}$

$$V_{REF} = \frac{R_2}{R_1 + R_2} V_{IN}(V), V_{OUT} \text{ track } V_{REF}$$

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