



-3.3A, -20V P-CHANNEL ENHANCEMENT MODE POWER MOSFET

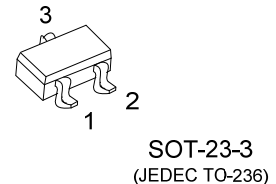
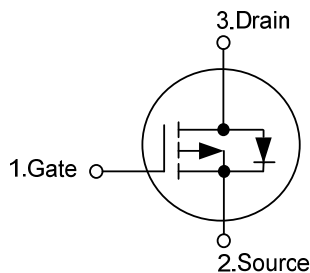
DESCRIPTION

The UTC **UT2315** is P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

FEATURES

- * Extremely low on-resistance due to high density cell
- * Perfect thermal performance and electrical capability with advanced technology of trench process

SYMBOL



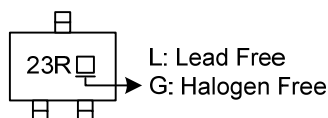
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT2315L-AE2-R	UT2315G-AE2-R	SOT-23-3	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

UT2315G-AE2-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) AE2: SOT-23-3
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 10	V
Continuous Drain Current	I_D	-3.3	A
Pulsed Drain Current	I_{DM}	-13.2	A
Peak Diode Recovery dv/dt (Note 4)	dv/dt	2.5	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$) (Note 3)	P_D	1.56	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. Surface mounted on 1 in 2 copper pad of FR4 board.

4. $I_{SD} \leq 3.3\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (PCB mounted)	θ_{JA}	80	$^\circ\text{C}/\text{W}$

Note: Surface Mounted on FR4 board $t \leq 5$ sec.

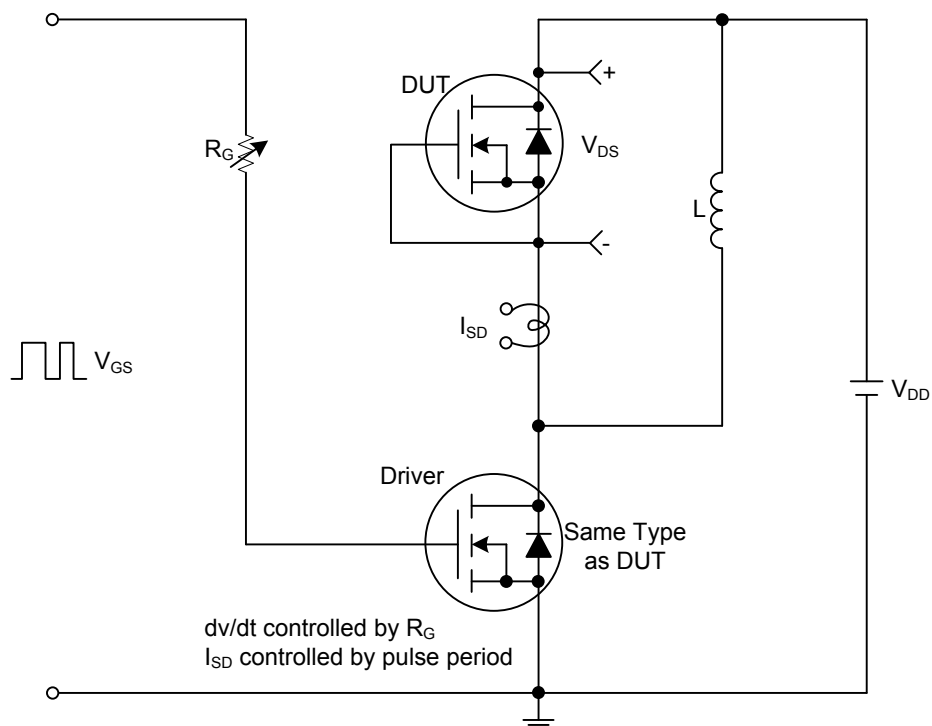
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-20			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V, T _J = 25°C			-1	μA
		V _{DS} =-16V, V _{GS} =0V, T _J = 125°C			-10	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-0.3	-0.6	-1.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-3.0A			82	mΩ
		V _{GS} =-2.5V, I _D =-2.6A			107	mΩ
		V _{GS} =-1.8V, I _D =-1.0A			150	mΩ
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S	V _G =V _D =0V , Force Current			-3.3	A
Maximum Body-Diode Pulsed Current	I _{SM}				-13.2	A
Drain-Source Diode Forward Voltage	V _{SD}	I _S =-1.0A, V _{GS} =0V, T _J = 25°C			-1.0	V

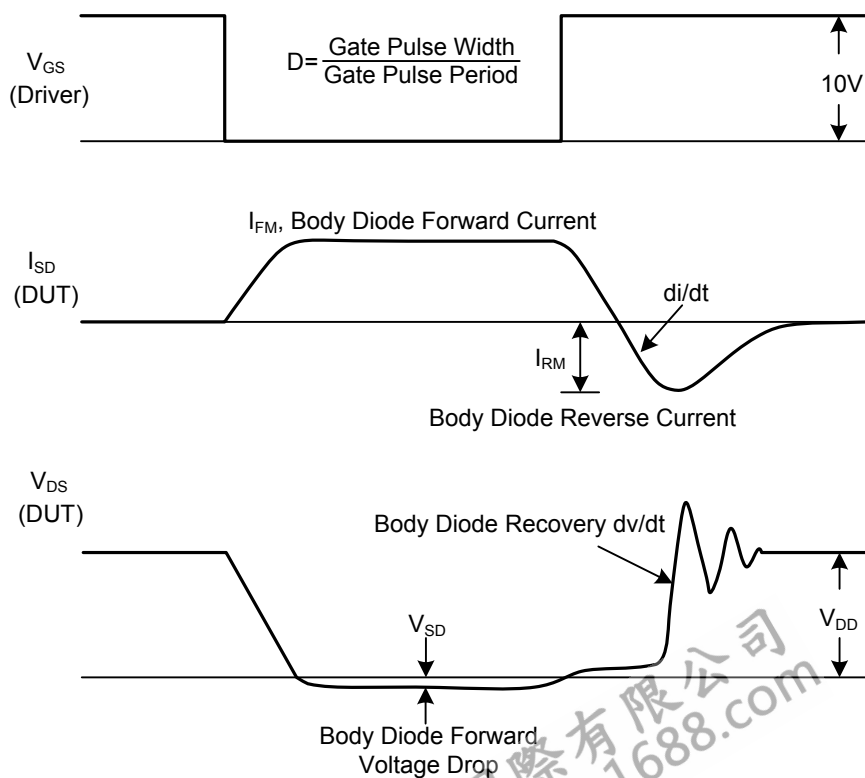
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



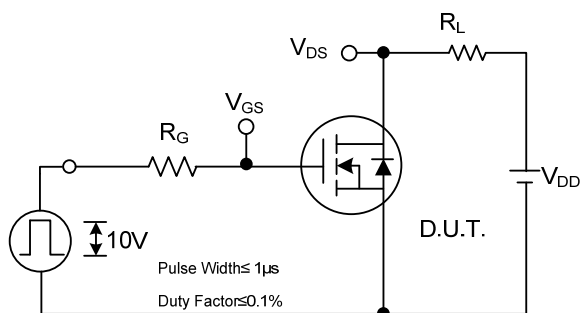
Peak Diode Recovery dv/dt Test Circuit



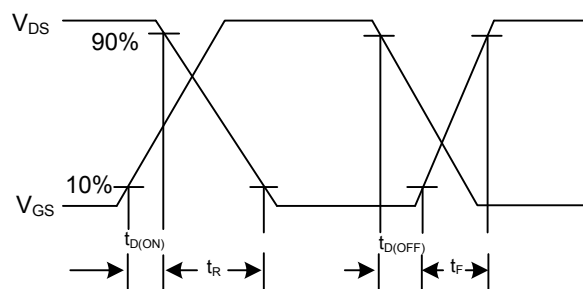
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

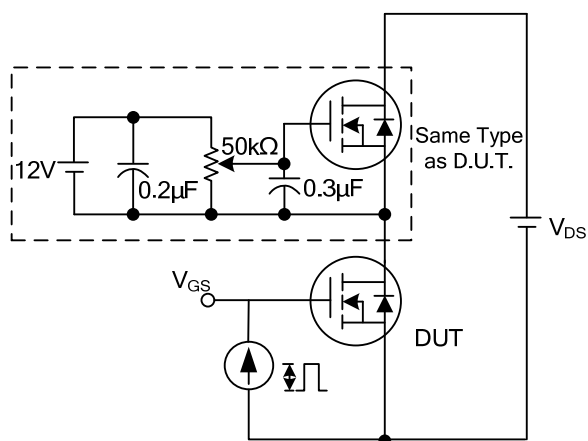
■ TEST CIRCUITS AND WAVEFORMS



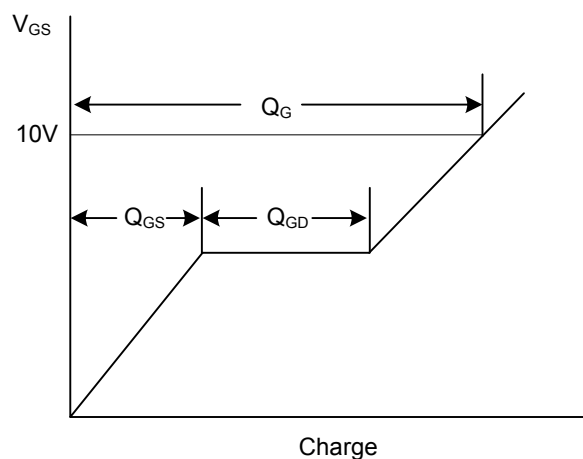
Switching Test Circuit



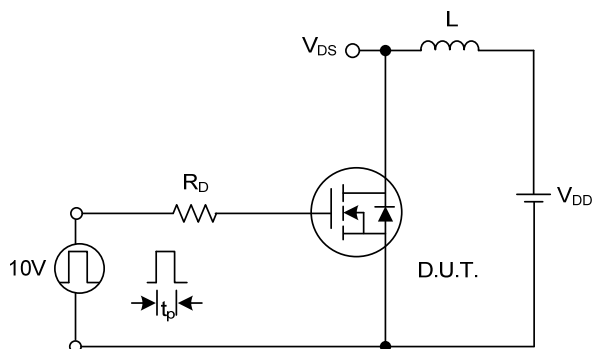
Switching Waveforms



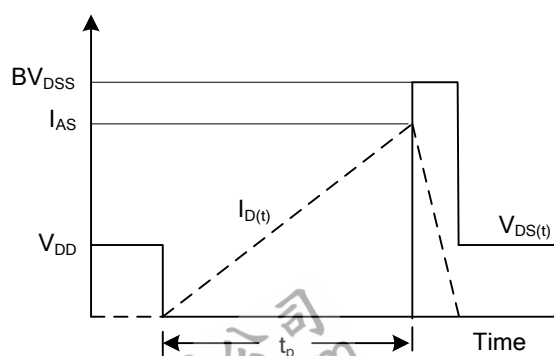
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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