



UT3008-H

Preliminary

Power MOSFET

-30V P-CHANNEL ENHANCEMENT MODE MOSFET

DESCRIPTION

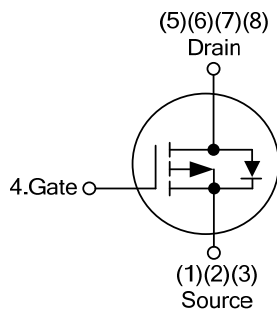
The UTC **UT3008-H** is a P-channel MOSFET, it uses UTC's advanced technology to provide the customers with a minimum on state resistance.

The UTC **UT3008-H** is suitable for backlighting, power management functions and DC-DC converters.

FEATURES

- * $R_{DS(ON)} < 17m\Omega @ V_{GS} = -10V, I_D = -10A$
- $R_{DS(ON)} < 25m\Omega @ V_{GS} = -4.5V, I_D = -10A$
- * Low $R_{DS(ON)}$

SYMBOL

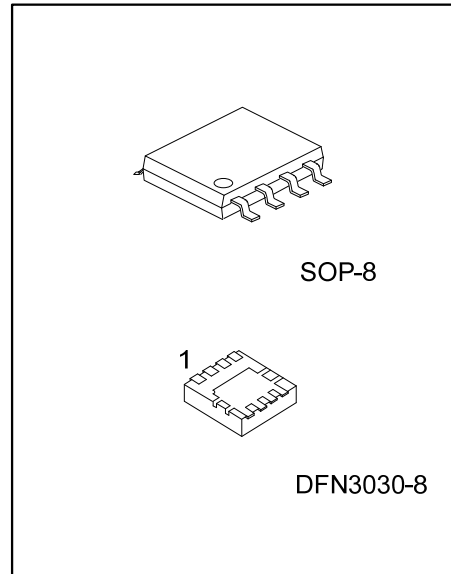


ORDERING INFORMATION

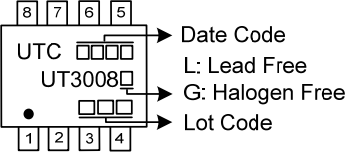
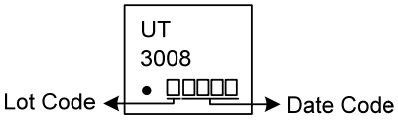
Ordering Number		Package	Pin Assignment						Packing		
Lead Free	Halogen Free		1	2	3	4	5	6		7	8
UT3008L-S08-R	UT3008G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT3008L-K08-3030-R	UT3008G-K08-3030-R	DFN3030-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT3008G-S08-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) S08: SOP-8, K08-3030: DFN3030-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

SOP-8	DFN3030-8
 <p>The diagram shows an SOP-8 package with pins numbered 1 to 8. The marking includes:<ul style="list-style-type: none">Top edge: 8, 7, 6, 5Bottom edge: 1, 2, 3, 4Top-left: UTCTop-center: UT3008Bottom-center: Lot Code (indicated by a dot and two boxes)Arrows point from the boxes to labels: 'Date Code' (for the top four boxes), 'L: Lead Free' and 'G: Halogen Free' (for the top-center text), and 'Lot Code' (for the bottom-center text).</p>	 <p>The diagram shows a DFN3030-8 package with the following marking:<ul style="list-style-type: none">Top-left: UTTop-center: 3008Bottom-center: Lot Code (indicated by a dot and two boxes)Arrows point from the boxes to labels: 'Lot Code' (for the bottom-center text) and 'Date Code' (for the top-center text).</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current (Note 2) ($T_A=25^\circ\text{C}$) $V_{GS}=-10\text{V}$		I_D	-11.7	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle=1%)		I_{DM}	-80	A
Maximum Continuous Body Diode Forward Current (Note 2)		I_S	-3.0	A
Total Power Dissipation	(Note 1)	SOP-8	1.4	W
		DFN3030-8	0.9	W
	(Note 2)	SOP-8	2.2	W
		DFN3030-8		W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Junction to Ambient (Note 1)	SOP-8	θ_{JA}	89	$^\circ\text{C/W}$
	DFN3030-8		140	$^\circ\text{C/W}$
Junction to Ambient (Note 2)	SOP-8		56	$^\circ\text{C/W}$
	DFN3030-8		57	$^\circ\text{C/W}$
Junction-to-Case (Note 2)	SOP-8	θ_{JC}	2.5	$^\circ\text{C/W}$
	DFN3030-8		7.1	$^\circ\text{C/W}$

Notes: 1. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PARAMETERS (Note 1)						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$			-1.0	μA
Gate-Source Leakage Current	Forward	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS (Note 1)						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.1	-1.6	-2.1	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10\text{V}$, $I_D=-10\text{A}$		12.5	17	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$, $I_D=-10\text{A}$		18.5	25	$\text{m}\Omega$
DYNAMIC PARAMETERS (Note 2)						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=-25\text{V}$, $f=1.0\text{MHz}$		880		pF
Output Capacitance	C_{OSS}			145		pF
Reverse Transfer Capacitance	C_{RSS}			140		pF
Gate Resistance	R_G	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$		6.4		Ω
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-0.5\text{A}$ $I_G=-100\mu\text{A}$		76.4		nC
Gate to Source Charge	Q_{GS}			4.8		nC
Gate to Drain Charge	Q_{GD}			3.6		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_G=6\Omega$ $I_D=-0.5\text{A}$		50		ns
Rise Time	t_R			49		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			460		ns
Fall-Time	t_F			230		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V_{SD}	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.7	-1.0	V

Notes: 1. Short duration pulse test used to minimize self-heating effect.

2. Guaranteed by design. Not subject to product testing.

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