



## UT40N04

Power MOSFET

### N-CHANNEL LOGIC LEVEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

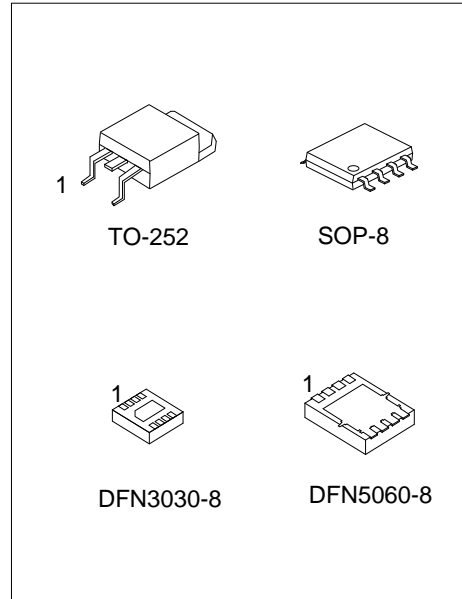
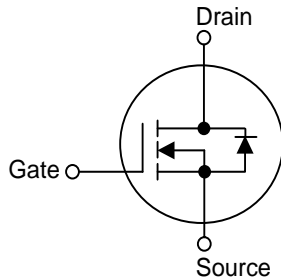
#### DESCRIPTION

The UTC **UT40N04** is an N-channel enhancement mode FET using advanced technology to provide fast switching speed, ruggedized device design, low on-resistance and cost-effectiveness.

#### FEATURES

- \* Low on-Resistance
- \* Fast Switching Speed

#### SYMBOL



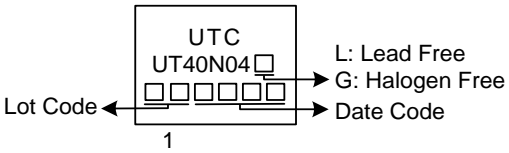
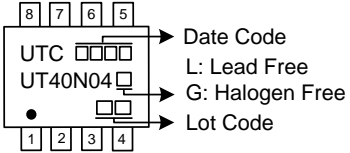
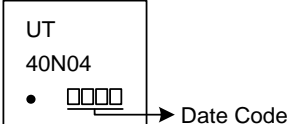
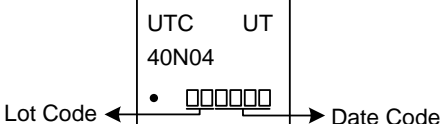
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT40N04L-TN3-R	UT40N04G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT40N04L-S08-R	UT40N04G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT40N04L-K08-3030-R	UT40N04G-K08-3030-R	DFN3030-8	S	S	S	G	D	D	D	D	Tape Reel
UT40N04L-K08-5060-R	UT40N04G-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT40N04G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252, S08: SOP-8, K08-3030: DFN3030-8 K08-5060: DFN5060-8</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

TO-252	SOP-8
 <p>UTC UT40N04 □ □□□□□ → Lot Code L: Lead Free G: Halogen Free □□□□ → Date Code 1</p>	 <p>8 7 6 5 UTC □□□□ → Date Code UT40N04 □ L: Lead Free G: Halogen Free • □□□ → Lot Code 1 2 3 4</p>
DFN3030-8	DFN5060-8
 <p>UT 40N04 • □□□□ → Date Code</p>	 <p>UTC UT 40N04 • □□□□□ → Lot Code □□□□ → Date Code</p>

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### ■ ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V <sub>DS</sub>	40	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	40	A
Pulsed Drain Current (Note 1)	I <sub>DM</sub>	80	A
Avalanche Energy	E <sub>AS</sub>	31.2	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	2.8	V/ns
Power Dissipation	TO-252	40	W
	SOP-8	6.25	W
	DFN3030-8	30	W
	DFN5060-8	35	W
Operating Junction Temperature	T <sub>J</sub>	-55 ~ +150	°C
Storage Temperature	T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. L=0.1mH, I<sub>AS</sub>=25A, V<sub>DD</sub>=20V, R<sub>G</sub>=25 Ω, Starting T<sub>J</sub> = 25°C

4. I<sub>SD</sub>≤30A, di/dt≤200A/μs, V<sub>DD</sub>≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C

### ■ THERMAL DATA (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	40	°C/W
	SOP-8	62.5	°C/W
	DFN3030-8	80	°C/W
	DFN5060-8	70	°C/W
Junction to Case	TO-252	3.125	°C/W
	SOP-8	20	°C/W
	DFN3030-8	4.16	°C/W
	DFN5060-8	3.57	°C/W

Notes: 1. Independent of Operating Temperature.

2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

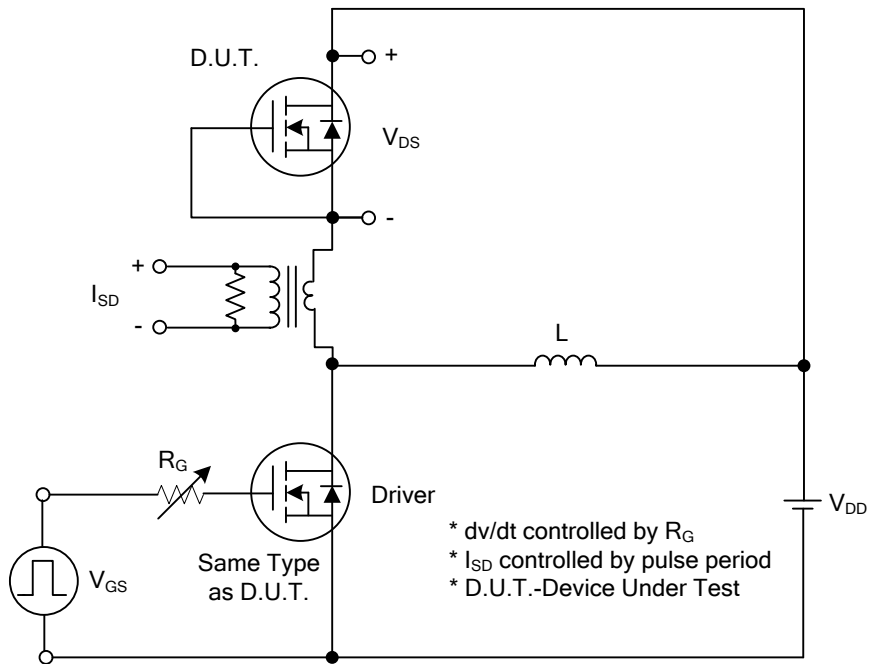
■ **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	40			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=40\text{V}$ , $V_{GS}=0\text{V}$			10	$\mu\text{A}$
Gate- Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance (Note 1)	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=20\text{A}$			12	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=10\text{A}$			16	$\text{m}\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		1230		pF
Output Capacitance	$C_{OSS}$			144		pF
Reverse Transfer Capacitance	$C_{RSS}$			122		pF
<b>SWITCHING PARAMETERS (Note 2)</b>						
Total Gate Charge	$Q_G$	$V_{DS}=20\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=40\text{A}$ , $I_G=1\text{mA}$ (Note1,2)		34.5		nC
	$Q_G$			17		nC
Gate to Source Charge	$Q_{GS}$	$V_{DS}=20\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=40\text{A}$ , $I_G=1\text{mA}$ (Note1,2)		6.6		nC
Gate to Drain Charge	$Q_{GD}$			7		nC
Turn-ON Delay Time	$t_{D(ON)}$			8.8		ns
Rise Time	$t_R$	$V_{DS}=20\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=40\text{A}$ , $R_G=25\Omega$ (Note1,2)		21		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			120		ns
Fall-Time	$t_F$			48		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$				40	A
Maximum Pulsed Drain-Source Diode Forward Current(Note 1)	$I_{SM}$				80	A
Drain-Source Diode Forward Voltage (Note 1)	$V_{SD}$	$I_F=40\text{A}$ , $V_{GS}=0\text{V}$			1.3	V

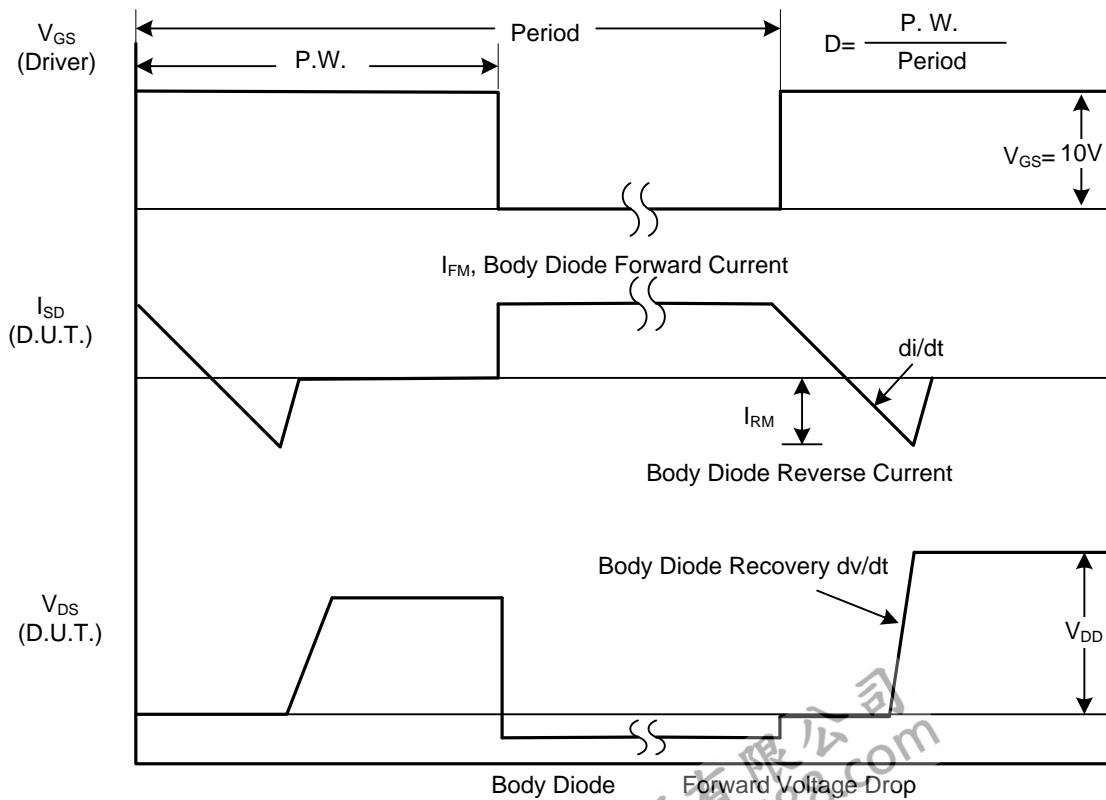
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

## TEST CIRCUITS AND WAVEFORMS

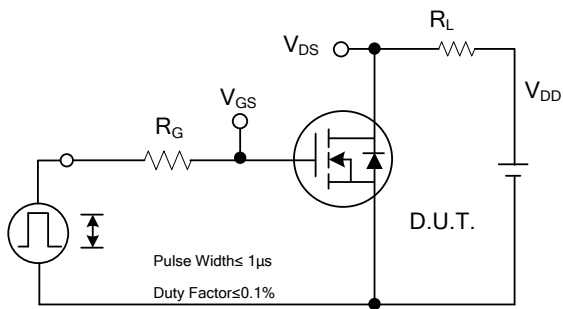


Peak Diode Recovery dv/dt Test Circuit

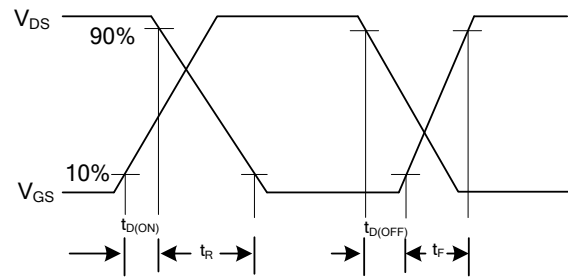


Peak Diode Recovery dv/dt Waveforms

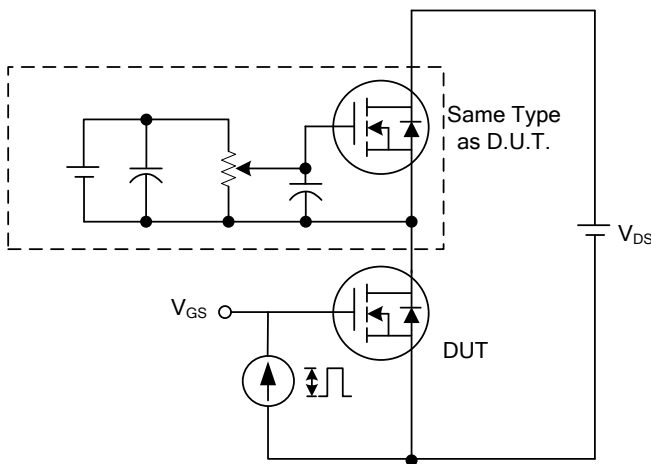
## TEST CIRCUITS AND WAVEFORMS



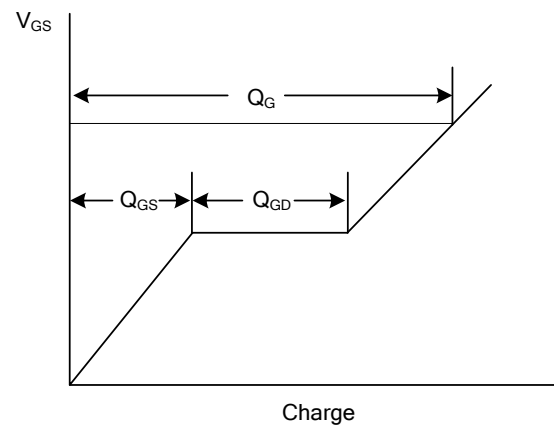
Switching Test Circuit



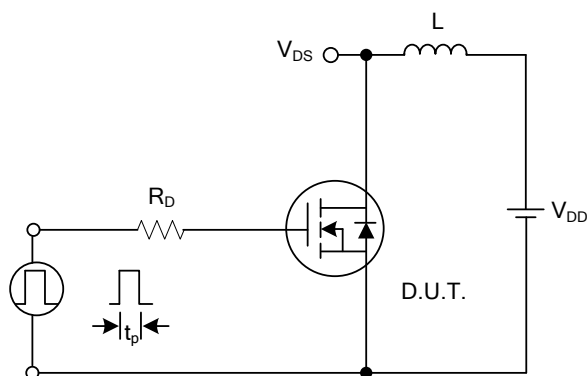
Switching Waveforms



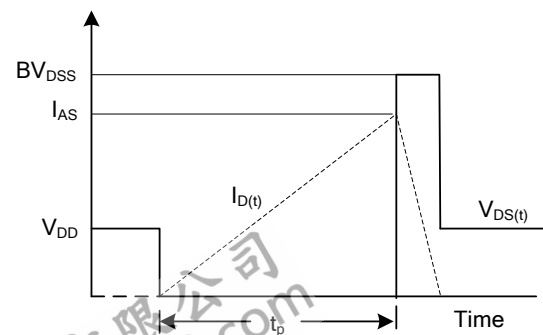
Gate Charge Test Circuit



Gate Charge Waveform

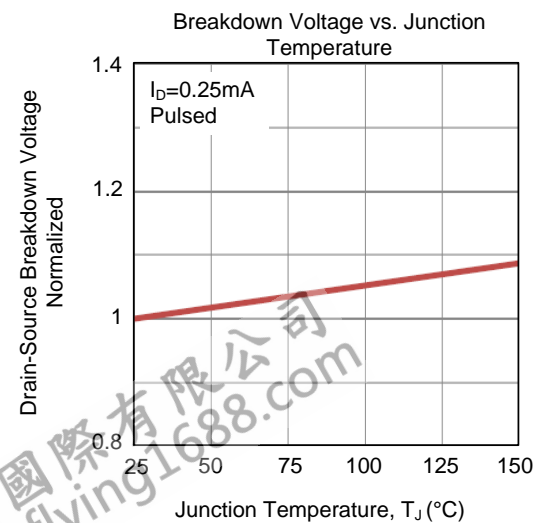
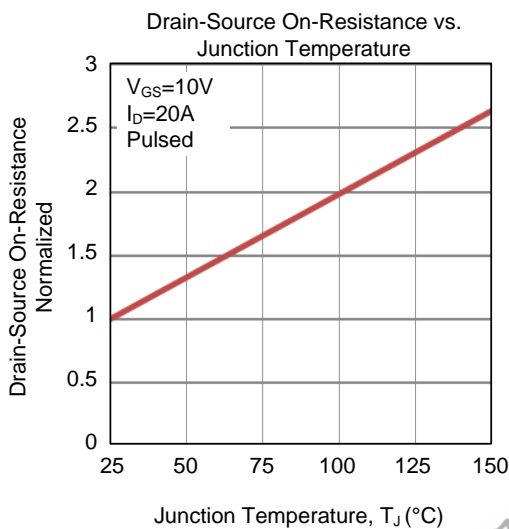
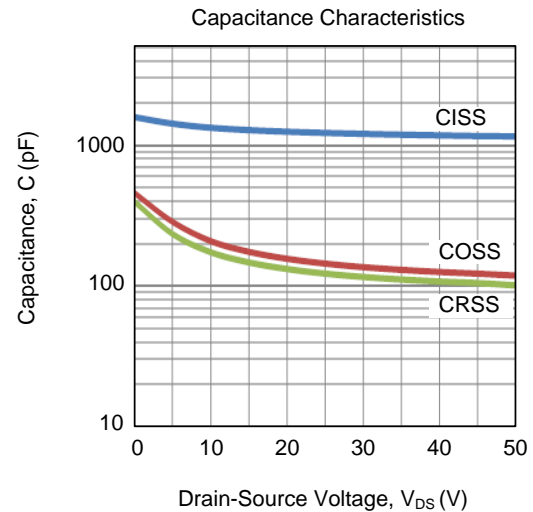
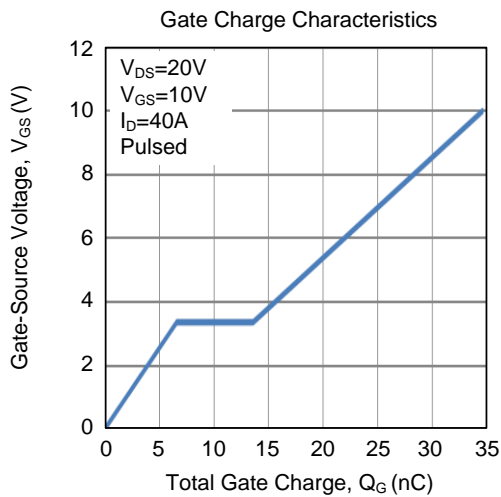
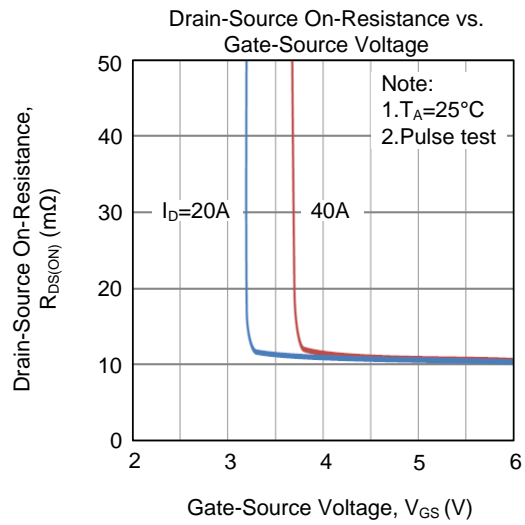
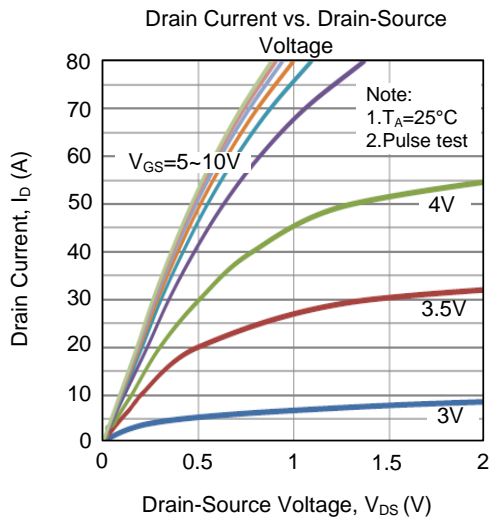


Unclamped Inductive Switching Test Circuit

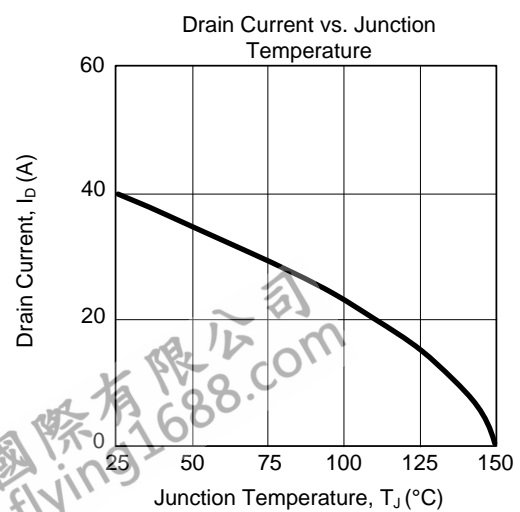
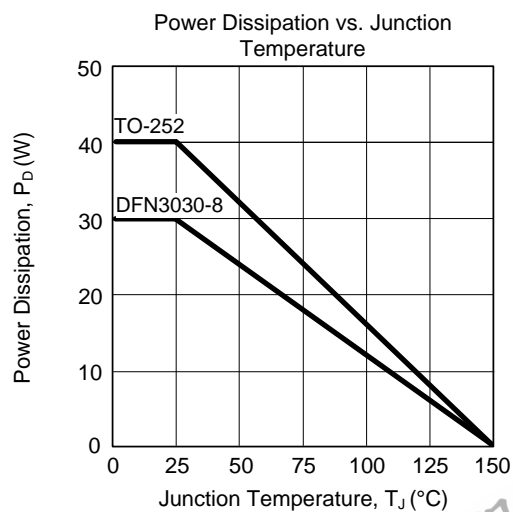
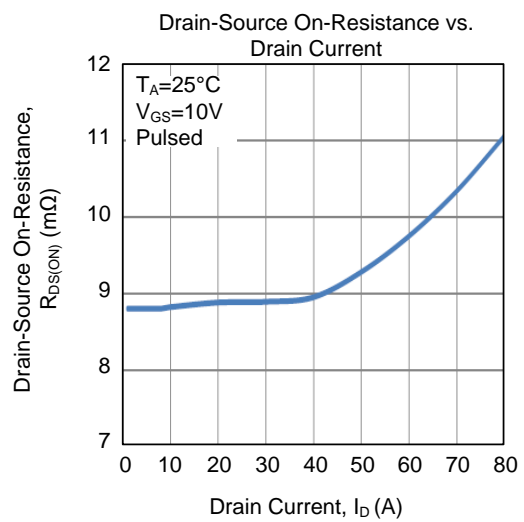
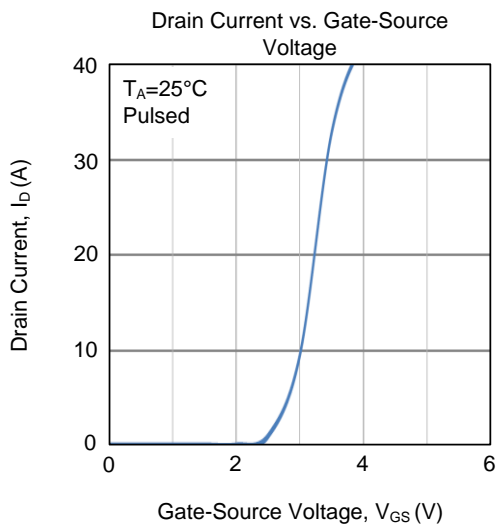
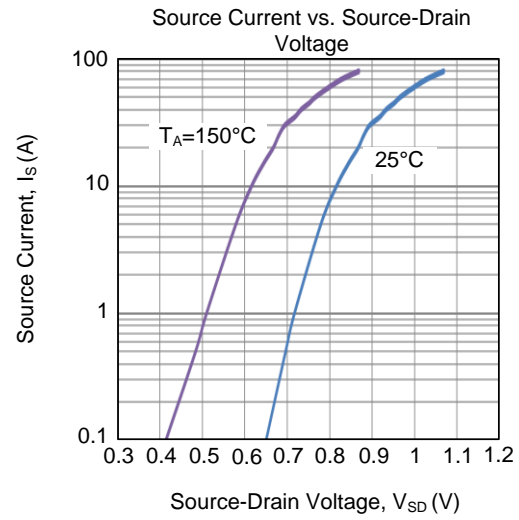
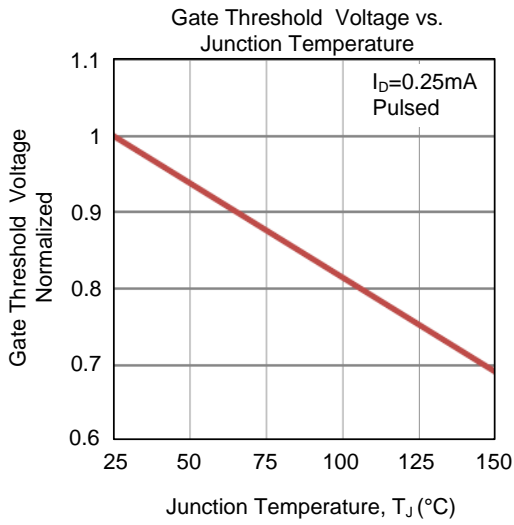


Unclamped Inductive Switching Waveforms

## TYPICAL CHARACTERISTICS

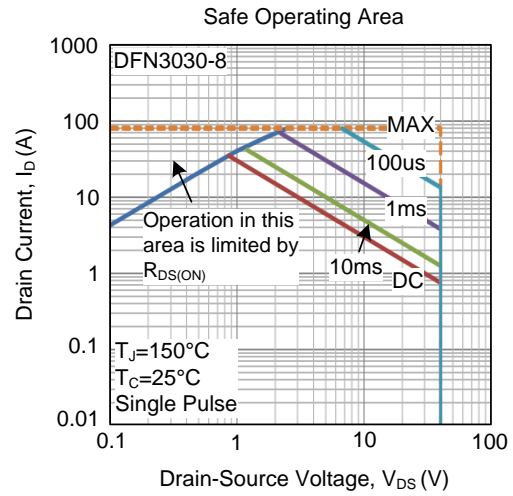
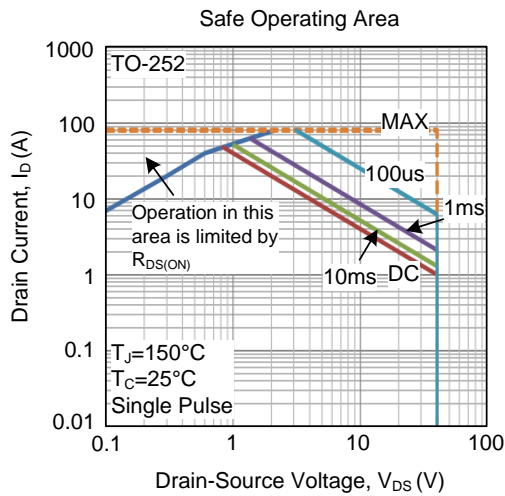


## ■ TYPICAL CHARACTERISTICS (Cont.)





### ■ TYPICAL CHARACTERISTICS (Cont.)



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