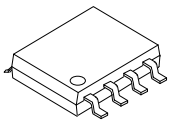
# -13A, -30V P-CHANNEL POWER MOSFET



SOP-8

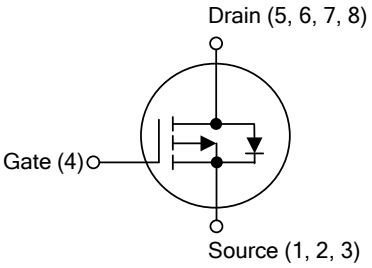
## ■ DESCRIPTION

UTC **UT4407** is a P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

## ■ FEATURES

* $R_{DS(ON)}$ < 9.5 mΩ @ $V_{GS}$=-10V, $I_D$=-10A
  $R_{DS(ON)}$ < 15 mΩ @ $V_{GS}$=-4.5V, $I_D$=-8.0A
* Improved dv/dt capability
* Fast switching

## ■ SYMBOL



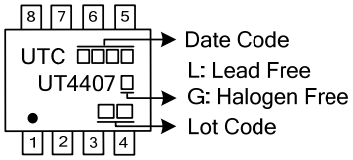

## ■ ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | | | | | | Packing |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Lead Free | Halogen Free | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| UT4407L-S08-R | UT4407G-S08-R | SOP-8 | S | S | S | G | D | D | D | D | Tape Reel |

Note: Pin Assignment: S: Source G: Gate D: Drain

| | |
|---|---|
| UT4407G-S08-R<br>(1)Packing Type | (1) R: Tape Reel |
| (2)Package Type | (2) S08: SOP-8 |
| (3)Green Package | (3) G: Halogen Free and Lead Free, L: Lead Free |

## ■ MARKING



## ■ ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25°C, unless otherwise specified)

| PARAMETER | | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DSS}$ | -30 | V |
| Gate-Source Voltage | | | $V_{GSS}$ | ±20 | V |
| Drain Current | Continuous | $T_C$ = 25°C | $I_D$ | -13 | A |
| | | $T_C$ = 100°C | | -7.8 | A |
| | Pulsed (Note 2) | | $I_{DM}$ | -52 | A |
| Power Dissipation | | | $P_D$ | 4.2 | W |
| Junction Temperature | | | $T_J$ | +150 | °C |
| Storage Temperature | | | $T_{STG}$ | -55 ~ +150 | °C |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L=0.1mH, $I_{AS}$=65A, $V_{DD}$=50V, $R_G$=25 Ω, Starting $T_J$ = 25°C

## ■ THERMAL DATA

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Junction to Ambient | $\theta_{JA}$ | 60 | °C/W |
| Junction to Case | $\theta_{JC}$ | 30 | °C/W |

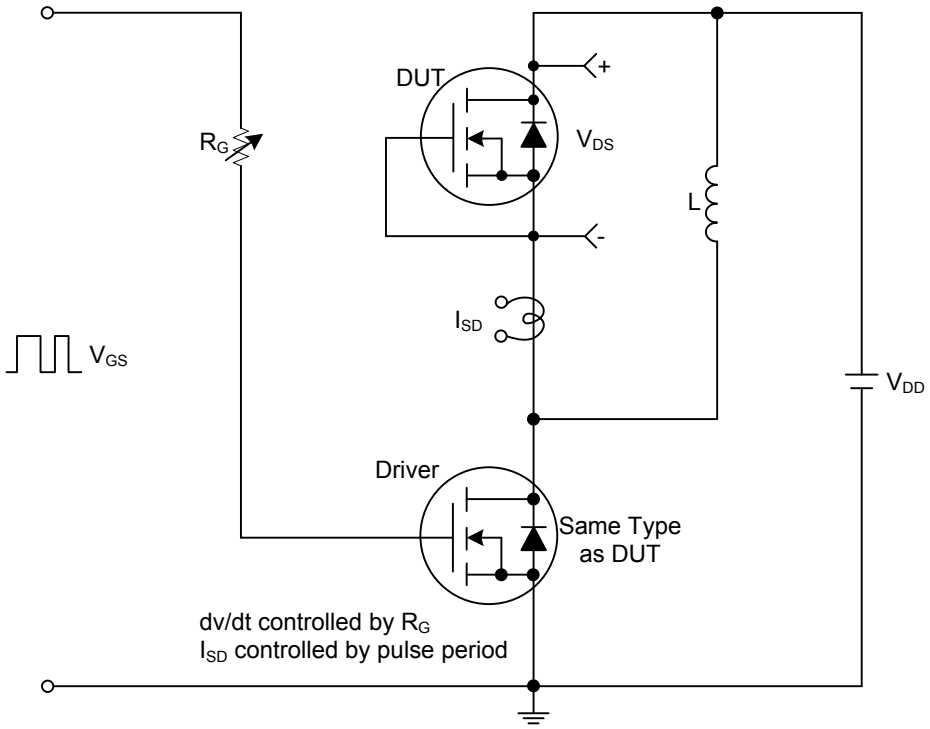
Note: The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.

## ■ ELECTRICAL CHARACTERISTICS ($T_J$ =25°C, unless otherwise specified)

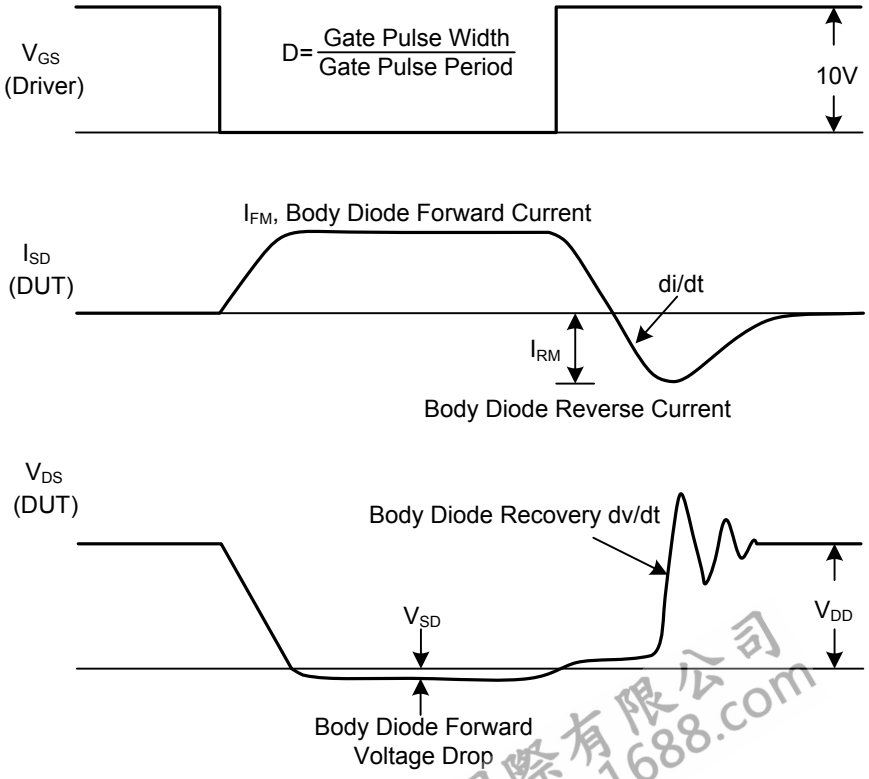
| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | $I_D$=250μA, $V_{GS}$=0V | -30 | | | V |
| $BV_{DSS}$ Temperature Coefficient | | $\triangle BV_{DSS}/\triangle T_J$ | Reference to 25°C , $I_D$=1mA | | -0.03 | | V/°C |
| Drain-Source Leakage Current | | $I_{DSS}$ | $V_{DS}$=-30V, $V_{GS}$=0V | | | -1 | μA |
| | | | $V_{DS}$=-24V, $V_{GS}$=0V | | | -10 | μA |
| Gate-Source Leakage Current | Forward | $I_{GSS}$ | $V_{GS}$=+20V, $V_{DS}$=0V | | | +100 | nA |
| | Reverse | | $V_{GS}$=-20V, $V_{DS}$=0V | | | -100 | nA |
| **ON CHARACTERISTICS** | | | | | | | |
| Gate Threshold Voltage | | $V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250μA | -1.0 | -1.6 | -2.5 | V |
| $V_{GS(TH)}$ Temperature Coefficient | | $\triangle V_{GS(TH)}$ | | | 4.0 | | mV/°C |
| Static Drain-Source On-State Resistance | | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=-10A | | 8.0 | 9.5 | mΩ |
| | | | $V_{GS}$=4.5V, $I_D$=-8.0A | | 12.4 | 15 | mΩ |
| Forward Transconductance | | gfs | $V_{DS}$=10V, $I_D$=-10A | | 13 | | S |
| **DYNAMIC PARAMETERS** | | | | | | | |
| Input Capacitance | | $C_{ISS}$ | $V_{GS}$=0V, $V_{DS}$=-15V, f=1.0MHz | | 3300 | 4800 | pF |
| Output Capacitance | | $C_{OSS}$ | | | 410 | 700 | pF |
| Reverse Transfer Capacitance | | $C_{RSS}$ | | | 280 | 500 | pF |
| Gate resistance | | $R_G$ | $V_{GS}$=0V, $V_{DS}$=0V, f=1.0MHz | | 8.5 | 12 | Ω |
| **SWITCHING PARAMETERS** | | | | | | | |
| Total Gate Charge (Note 1) | | $Q_G$ | $V_{DS}$=-15V, $V_{GS}$=-4.5V, $I_D$=-10A | | 35 | 56 | nC |
| Gate to Source Charge | | $Q_{GS}$ | | | 10.8 | 16 | nC |
| Gate to Drain Charge | | $Q_{GD}$ | | | 10.6 | 16 | nC |
| Turn-on Delay Time (Note 1) | | $t_{D(ON)}$ | $V_{DD}$=-15V, $V_{GS}$=-10V, $I_D$=-1.0A, $R_G$=6.0Ω | | 24.5 | 38 | ns |
| Rise Time | | $t_R$ | | | 10.5 | 16 | ns |
| Turn-off Delay Time | | $t_{D(OFF)}$ | | | 156.8 | 230 | ns |
| Fall-Time | | $t_F$ | | | 50 | 75 | ns |
| **SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS** | | | | | | | |
| Maximum Body-Diode Continuous Current | | $I_S$ | $V_G$=$V_D$=0V , Force Current | | | -13 | A |
| Maximum Body-Diode Pulsed Current | | $I_{SM}$ | | | | -26 | A |
| Drain-Source Diode Forward Voltage (Note 1) | | $V_{SD}$ | $I_S$=-1.0A, $V_{GS}$=0V | | | -1.0 | V |

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle≤2%.
2. Essentially independent of operating temperature.

## ■ TEST CIRCUITS AND WAVEFORMS



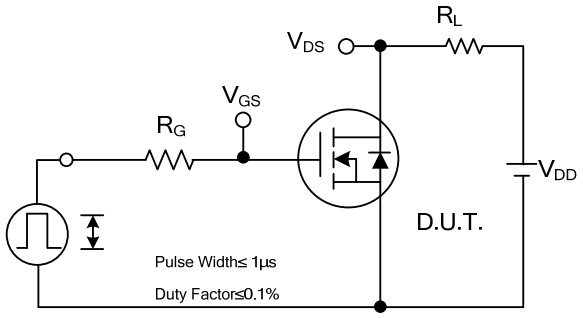

**Peak Diode Recovery dv/dt Test Circuit**



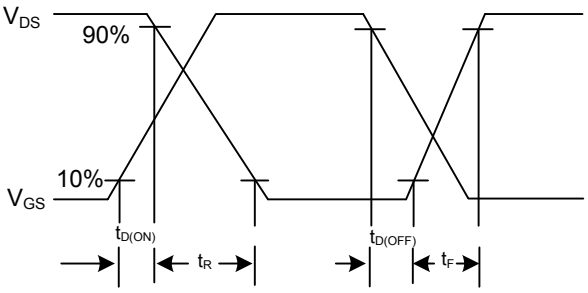

Peak Diode Recovery dv/dt Test Circuit and Waveforms

**Peak Diode Recovery dv/dt Waveforms**

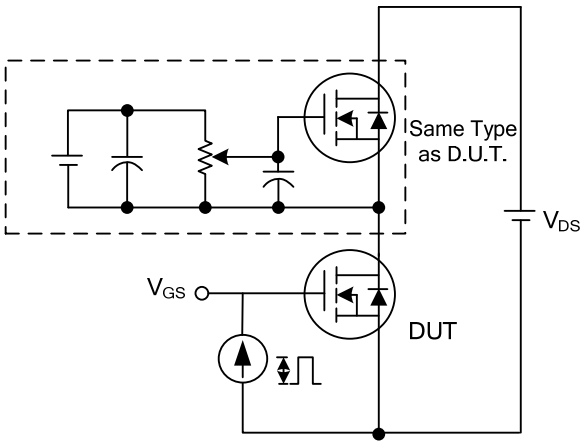
## ■ TEST CIRCUITS AND WAVEFORMS



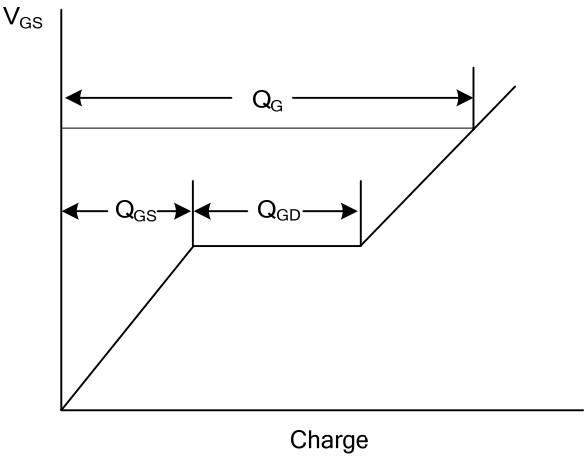

**Switching Test Circuit**



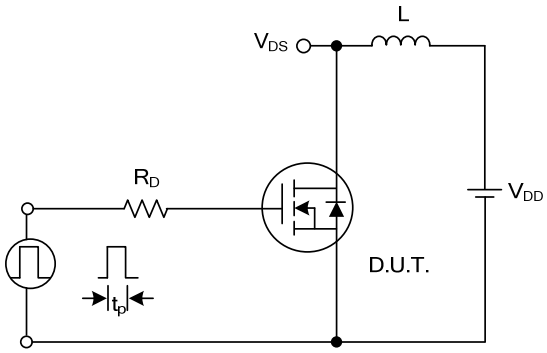

**Switching Waveforms**



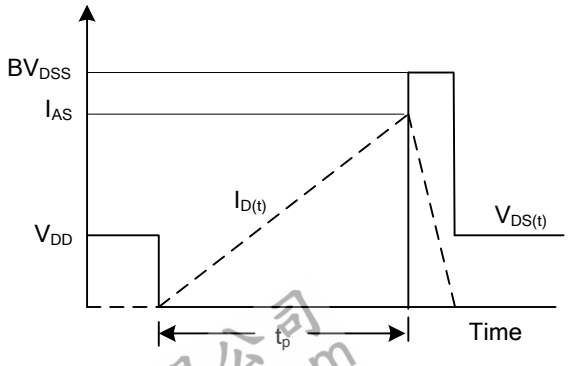

**Gate Charge Test Circuit**




**Gate Charge Waveform**




**Unclamped Inductive Switching Test Circuit**




**Unclamped Inductive Switching Waveforms**