



UT4435

Power MOSFET

-8.8A, -30V P-CHANNEL POWER MOSFET

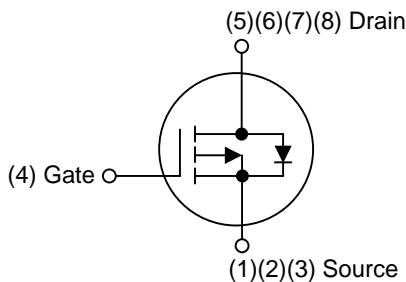
DESCRIPTION

The **UT4435** uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

FEATURES

- * $R_{DS(ON)} \leq 20\text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -8.8\text{A}$
- * $R_{DS(ON)} \leq 35\text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -6.7\text{A}$
- * Low capacitance
- * Low gate charge
- * Fast switching capability
- * Avalanche energy specified

SYMBOL

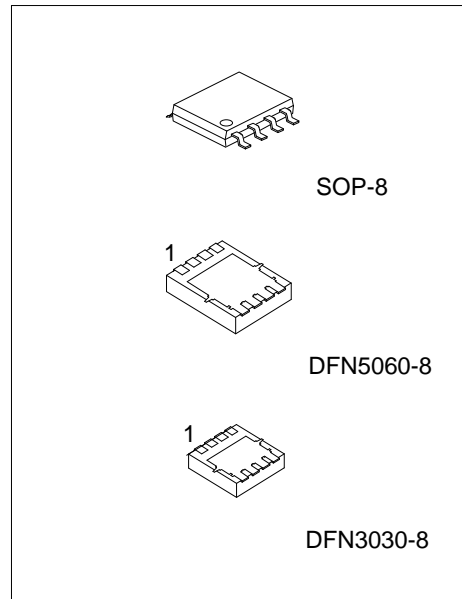


ORDERING INFORMATION

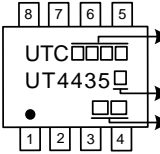
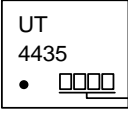
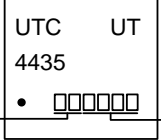
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT4435L-S08-R	UT4435G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT4435L-K08-3030-R	UT4435G-K08-3030-R	DFN3030-8	S	S	S	G	D	D	D	D	Tape Reel
UT4435L-K08-5060-R	UT4435G-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT4435G-S08-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8, K08-5060: DFN5060-8, K08-3030: DFN3030-8</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

PACKAGE	MARKING
SOP-8	 <p> UTC □ □ □ □ → Date Code L: Lead Free G: Halogen Free UT4435 □ → • □ □ → Lot Code </p>
DFN3030-8	 <p> UT 4435 • □ □ □ → Date Code </p>
DFN5060-8	 <p> UTC UT 4435 • □ □ □ □ □ → Date Code Lot Code ← </p>

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■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

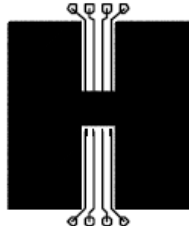
PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V _{DSS}	-30	V
Gate-Source Voltage	V _{GSS}	±25	V
Continuous Drain Current (Note 3a)	I _D	-8.8	A
Pulsed Drain Current	I _{DM}	-50	A
Power Dissipation (Note 3b)	SOP-8	1	W
	DFN3030-8	1.13	W
	DFN5060-8	1.56	W
Junction Temperature	T _J	+150	°C
Storage Temperature	T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

3. θ_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. θ_{JC} is guaranteed by design while θ_{JA} is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad.

■ THERMAL CHARACTERISTICS

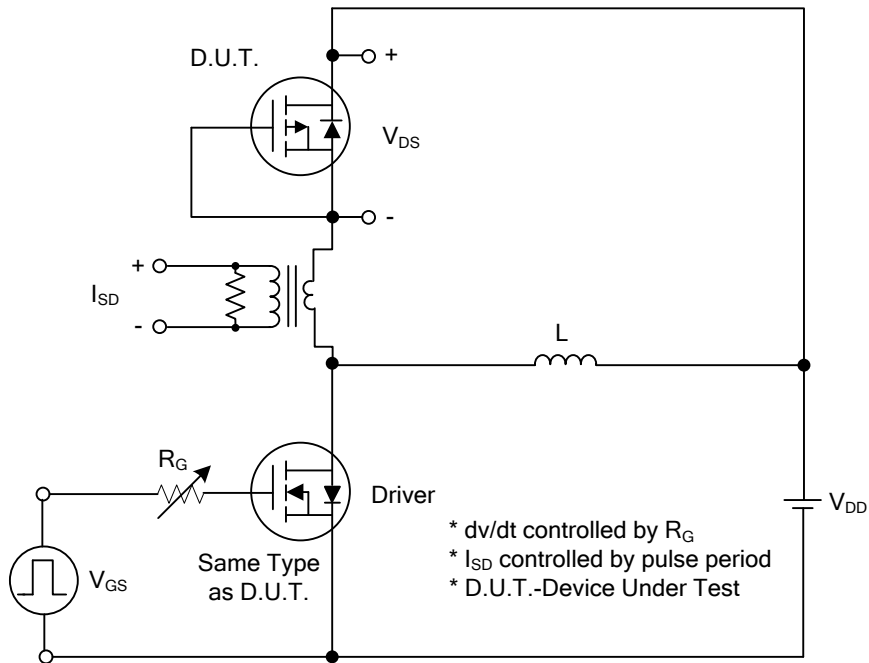
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 3a)	SOP-8	50	°C/W
	DFN3030-8	45	°C/W
	DFN5060-8	42.5	°C/W
Junction to Ambient(Note 3b)	SOP-8	125	°C/W
	DFN3030-8	110	°C/W
	DFN5060-8	80	°C/W
Junction to Case	SOP-8	25	°C/W
	DFN3030-8	13	°C/W
	DFN5060-8	3.5	°C/W

■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$, unless otherwise specified)

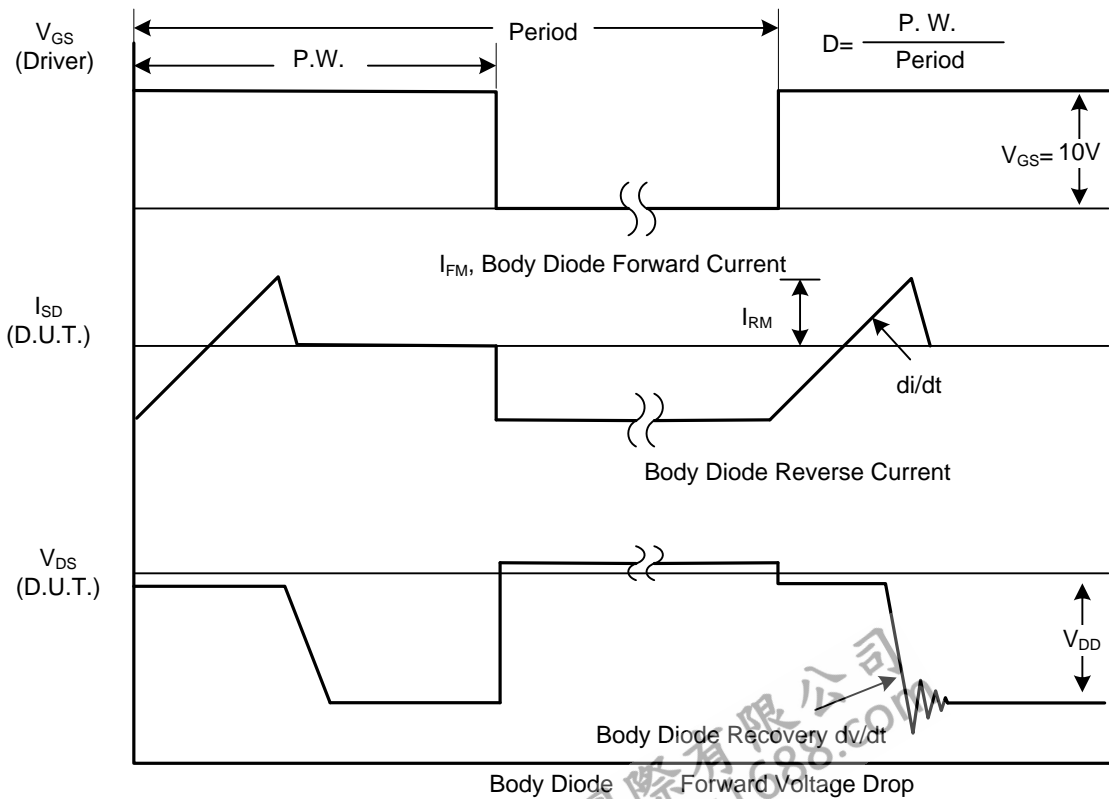
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$			-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$			± 100	nA
ON CHARACTERISTICS (Note)						
Gate-Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-1.0	-1.7	-3.0	V
On State Drain Current	$I_{D(ON)}$	$V_{GS}=-10V, V_{DS}=-5V$	-50			A
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-8.8A$		16.5	20	m Ω
		$V_{GS}=-4.5V, I_D=-6.7A$		26	35	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-8.8A$		24		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=-15V, V_{GS}=0V, f=1.0MHz$		2000		pF
Output Capacitance	C_{OSS}			285		pF
Reverse Transfer Capacitance	C_{RSS}			220		pF
SWITCHING PARAMETERS (Note)						
Total Gate Charge	Q_G	$V_{DS}=-15V, V_{GS}=-5V, I_D=-8.8A$		23	26	nC
Gate-Source Charge	Q_{GS}			5		nC
Gate-Drain Charge	Q_{GD}			6		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=-15V, I_D=-1A, V_{GS}=-10V$ $R_G=6\Omega$		15	23	ns
Turn-ON Rise Time	t_R			15.2	24	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			75	95	ns
Turn-OFF Fall-Time	t_F			38	50	ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Maximum Body-Diode Continuous Current	I_S				-2.1	A
Diode Forward Voltage(Note)	V_{SD}	$I_S=-2.1A, V_{GS}=0V$			1.4	V

Note: Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%.

■ TEST CIRCUITS AND WAVEFORMS

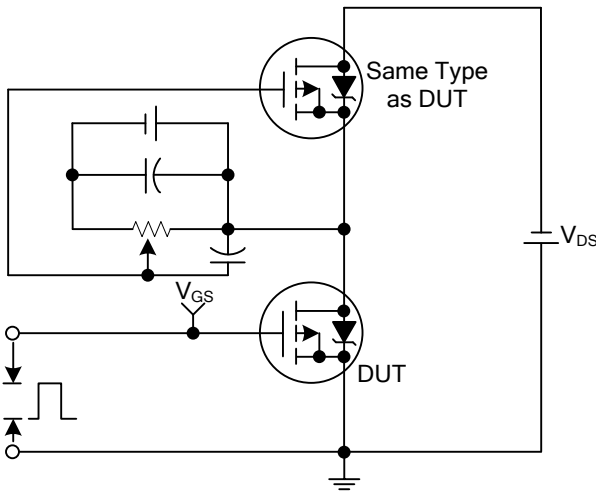


Peak Diode Recovery dv/dt Test Circuit

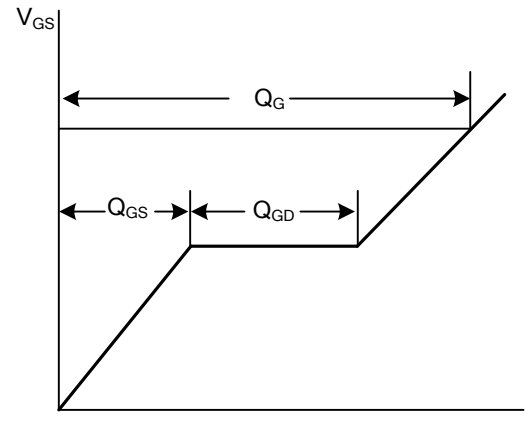


Peak Diode Recovery dv/dt Waveforms

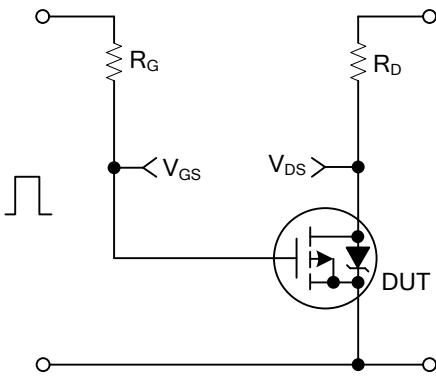
■ TEST CIRCUITS AND WAVEFORMS



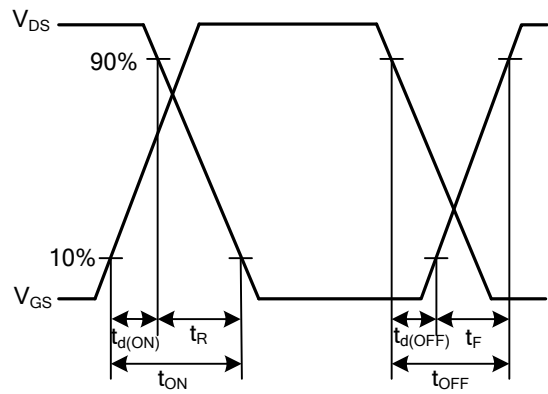
Gate Charge Test Circuit



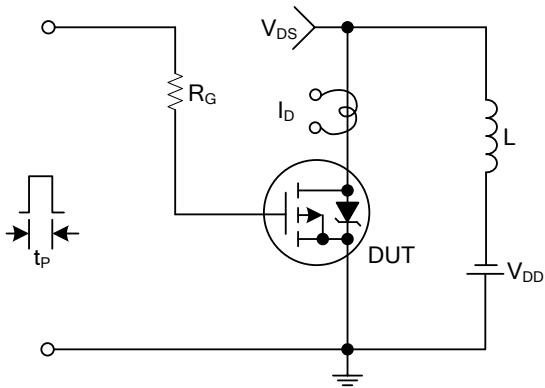
Gate Charge Waveforms



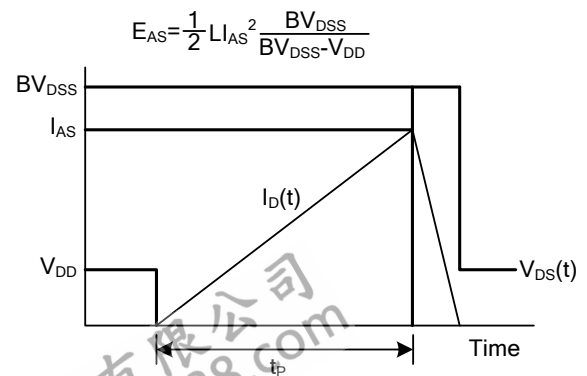
Resistive Switching Test Circuit



Resistive Switching Waveforms

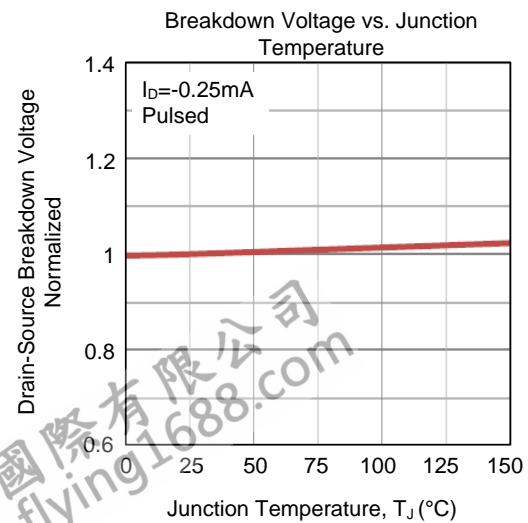
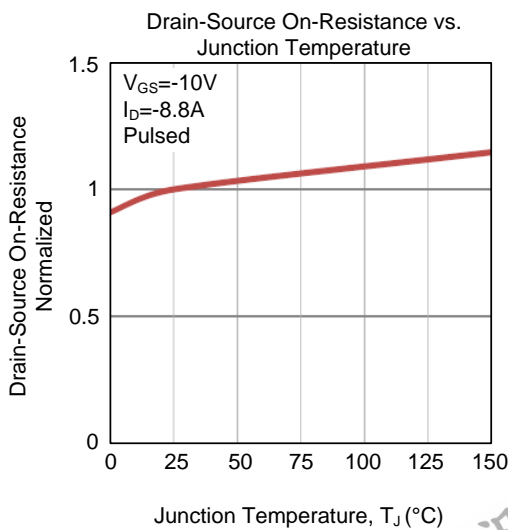
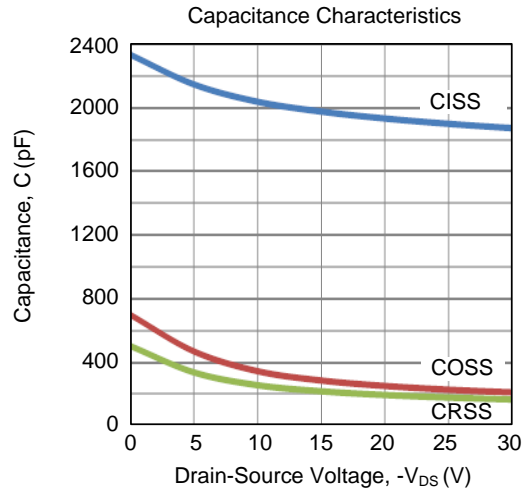
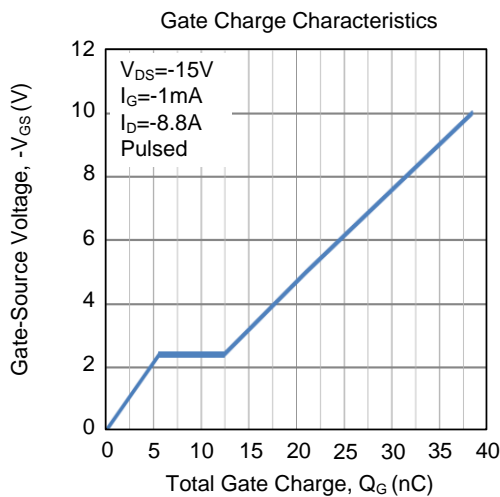
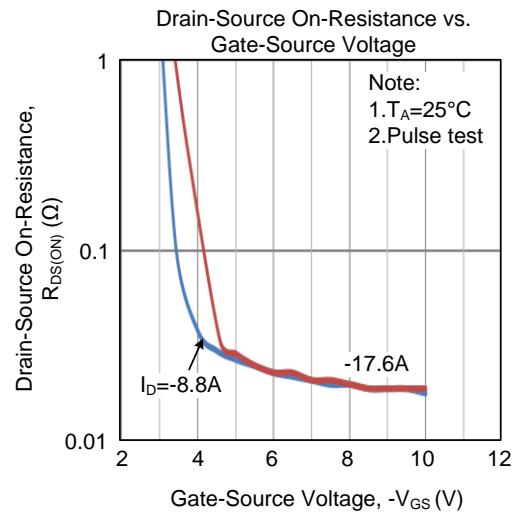
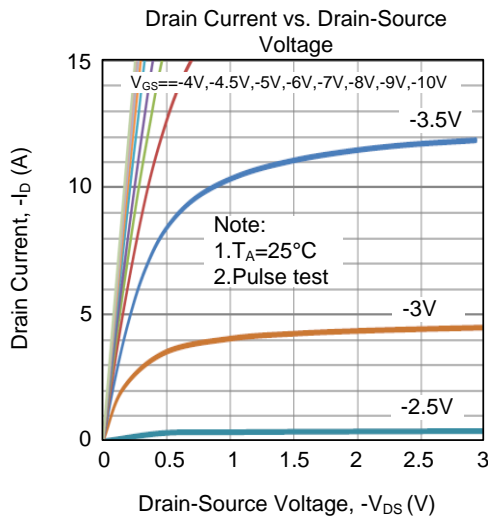


Unclamped Inductive Switching Test Circuit

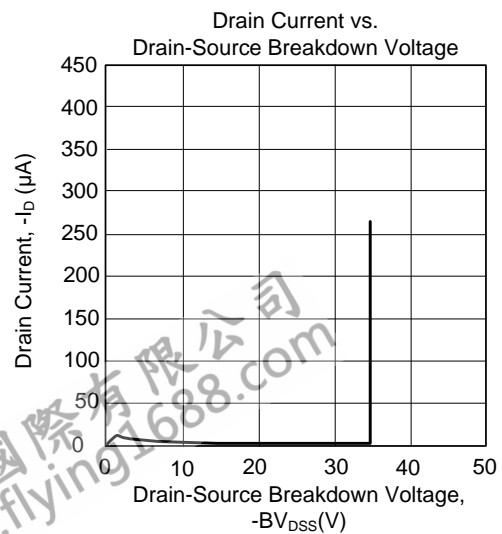
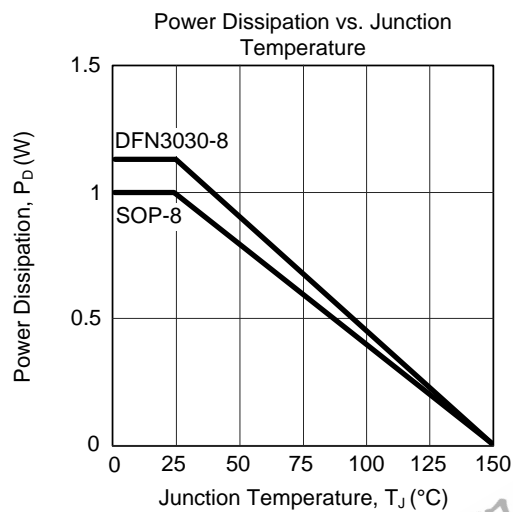
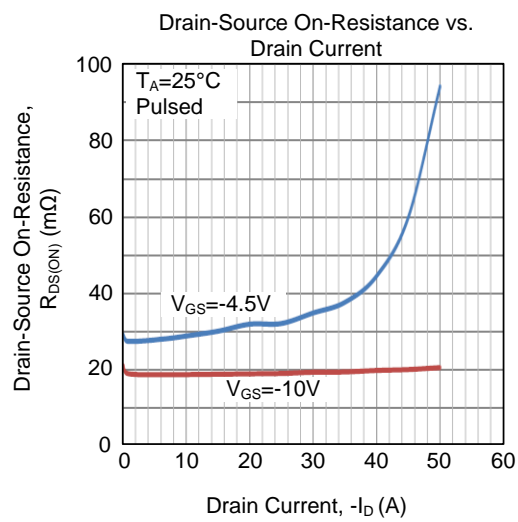
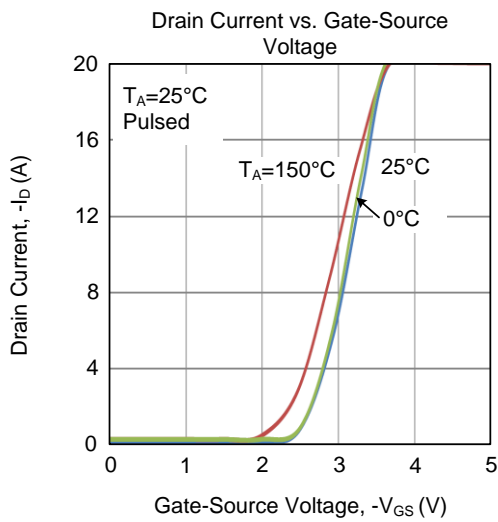
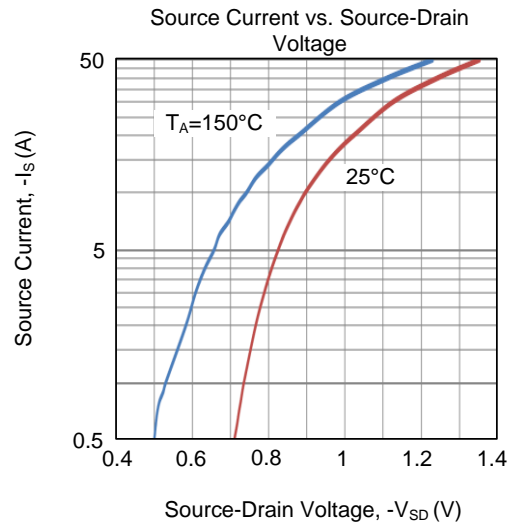
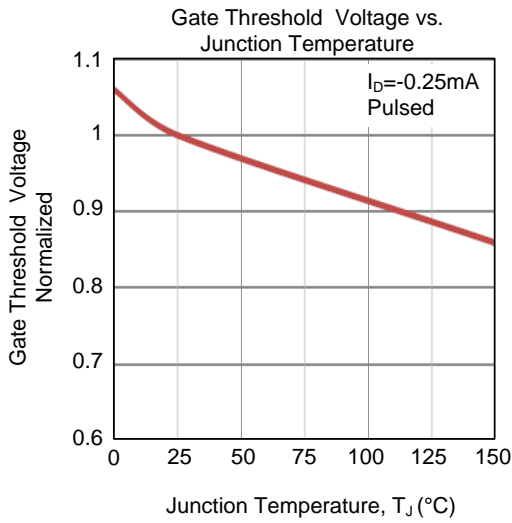


Unclamped Inductive Switching Waveforms

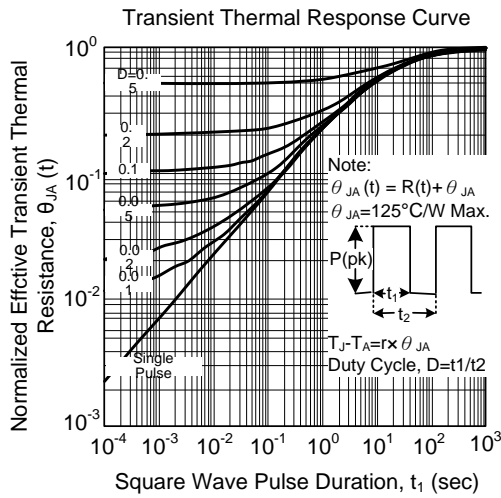
■ TYPICAL CHARACTERISTICS



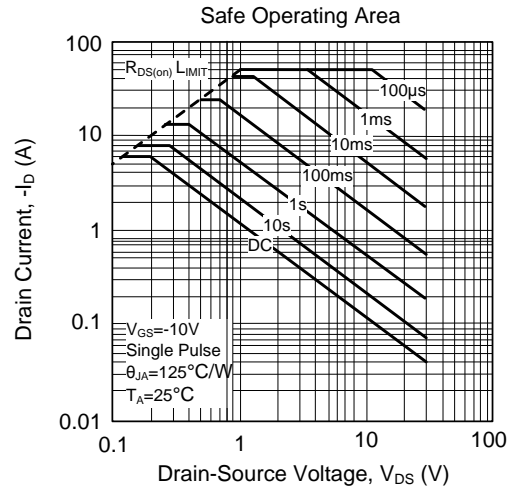
■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



Thermal characterization performed using the conditions described in Note 3b. Transient thermal response will change depending on the circuit board design.



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