# UNISONIC TECHNOLOGIES CO., LTD

UT45N02 Power MOSFET

# 45A, 20V **N-CHANNEL** POWER MOSFET

#### **DESCRIPTION**

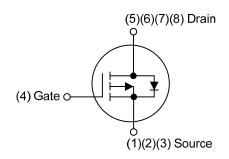
The UTC UT45N02 is a N-channel power MOSFET providing very low on-resistance. It has high efficiency and perfect cost-effectiveness. This device is ideal for load switch and battery protection applications. For example in applications such as switching regulators, switching converters, motor drivers and relay drivers.

These transistors can be operated directly from integrated circuits, applied in the commercial and industrial fields.

#### **FEATURES**

- \*  $R_{DS(on)} \le 12m\Omega$  @  $V_{GS}=10V$ ,  $I_{D}=22.5A$  $R_{DS(on)} \le 14m\Omega @ V_{GS} = 4.5V, I_D = 22.5A$
- \* High breakdown voltage

## **SYMBOL**



## ORDERING INFORMATION

Note: Pin Assignment: G: Gate

Ordering Number		Daalaasa	Pin Assignment							Daaliaa	
Lead Free	Halogen Free	Package	1	2	3	4	5	6	7	8	Packing
UT45N02L-S08-R	UT45N02G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

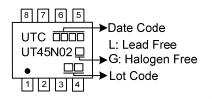
UT45N02G-S08-R (1)Packing Type (1) R: Tape Reel (2)Package Type (2) S08: SOP-8 (3) G: Halogen Free and Lead Free L: Lead Free

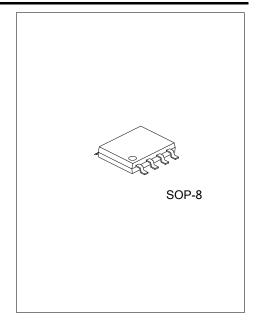
S: Source

D: Drain

(3)Green Package

#### **MARKING**





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## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> =25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	20	V
Gate-Source Voltage		$V_{GSS}$	±8	V
Drain Current	Continuous	I <sub>D</sub>	45	Α
	Pulsed	I <sub>DM</sub>	90	Α
Single Pulsed Avalanche Energy (Note 3)		E <sub>AS</sub>	67.3	mJ
Power Dissipation		P <sub>D</sub>	6	W
Junction Temperature		TJ	+150	°C
Storage Temperature Range		T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3. L=0.1mH,  $I_{AS}$ =36.7A,  $V_{DD}$ =20V,  $R_{G}$ =25  $\Omega$ , Starting  $T_{J}$  = 25°C

#### THERMAL DATA

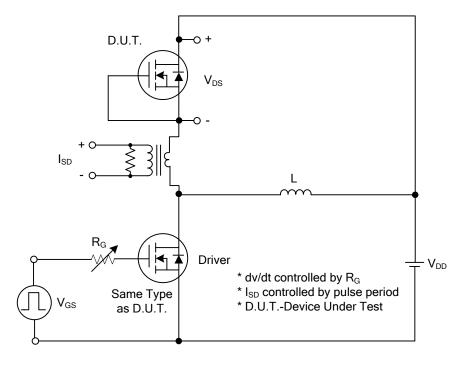
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	125	°C/W
Junction to Case	$\theta_{JC}$	20.8 (Note)	°C/W

Note: Device mounted on FR-4 substrate Pc board, 2oz copper, with 1inch square copper plate.

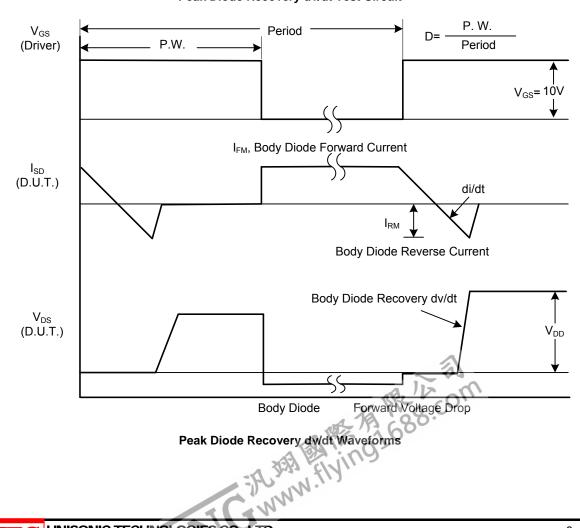
#### ELECTRICAL CHARACTERISTICS (T<sub>C</sub> =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
OFF CHARACTERISTICS									
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	20			V		
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	μΑ		
Gate-Source Leakage Current	Forward		V <sub>GS</sub> =+10V, V <sub>DS</sub> =0V			+100	nA		
	Reverse	$I_{GSS}$	V <sub>GS</sub> =-10V, V <sub>DS</sub> =0V			-100	nA		
ON CHARACTERISTICS									
Gate Threshold Voltage		$V_{GS(TH)}$	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.4		1.0	V		
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A		7.2	9	mΩ		
			V <sub>GS</sub> =2.5V, I <sub>D</sub> =6.0A		11.7	14.5	mΩ		
DYNAMIC PARAMETERS									
Input Capacitance		C <sub>ISS</sub>			1250		рF		
Output Capacitance	Output Capacitance		$V_{GS}$ =0V, $V_{DS}$ =20V, f=1.0MHz		236		pF		
Reverse Transfer Capacitance		C <sub>RSS</sub>			222		pF		
SWITCHING PARAMETERS									
Total Gate Charge		$Q_G$	\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		23		nC		
Gate to Source Charge		$Q_GS$	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =45A,		2.3		nC		
Gate to Drain Charge		$Q_{GD}$	I <sub>D</sub> =1mA (Note 1, 2)		7.5		nC		
Turn-ON Delay Time		t <sub>D(ON)</sub>			6		ns		
Rise Time		t <sub>R</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =45A,		17		ns		
Turn-OFF Delay Time		t <sub>D(OFF)</sub>	R <sub>G</sub> =25Ω (Note 1, 2)		42		ns		
Fall-Time		t <sub>F</sub>			22		ns		
SOURCE- DRAIN DIODE RATING	SS AND CI	HARACTERI	STICS						
Maximum Body-Diode Continuous Current		Is	~ 01			45	Α		
Maximum Body-Diode Pulsed Cur	rent	I <sub>SM</sub>	WE TON			90	Α		
Drain-Source Diode Forward Volta	ige	$V_{SD}$	I <sub>S</sub> =1.0A, V <sub>GS</sub> =0V	1.2	V				
Notes: 1. Pulse Test: Pulse width ≤ 300us. Duty cycle < 2%									
Essentially independent of operating temperature.									
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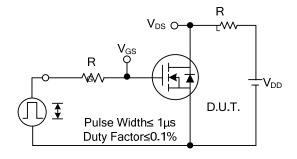
## **TEST CIRCUITS AND WAVEFORMS**



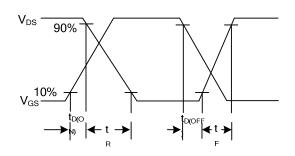
## Peak Diode Recovery dv/dt Test Circuit



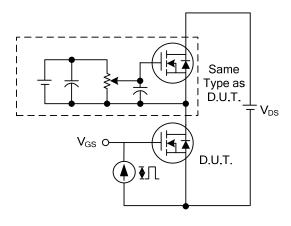
## **TEST CIRCUITS AND WAVEFORMS**



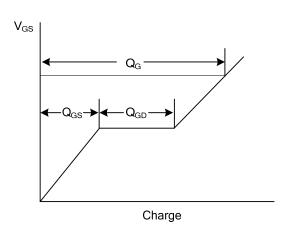
**Switching Test Circuit** 



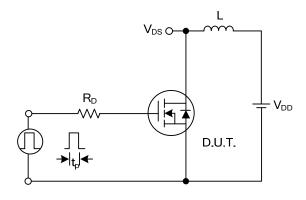
Switching Waveforms



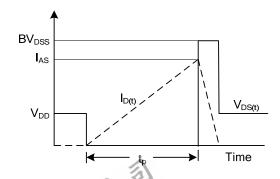
Gate Charge Test Circuit



Gate Charge Waveform

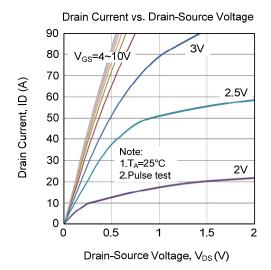


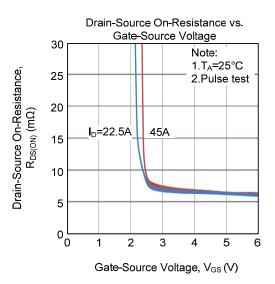
**Unclamped Inductive Switching Test Circuit** 

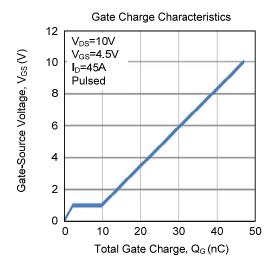


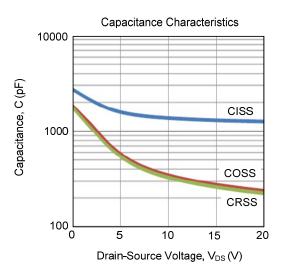
Unclamped Inductive Switching Waveforms

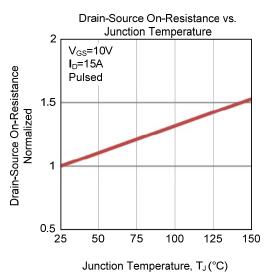
#### **■ TYPICAL CHARACTERISTICS**

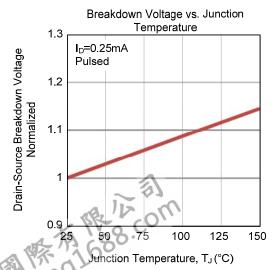




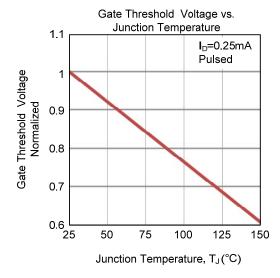


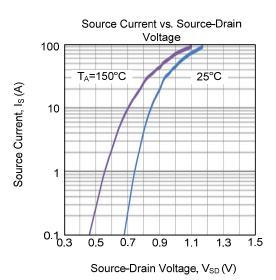


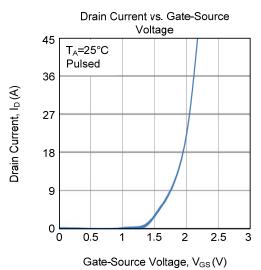


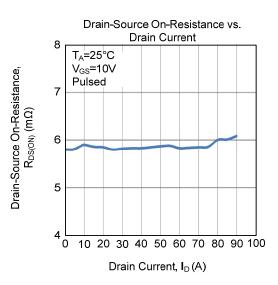


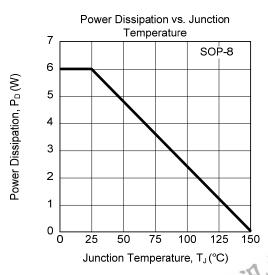
## **■ TYPICAL CHARACTERISTICS (Cont.)**

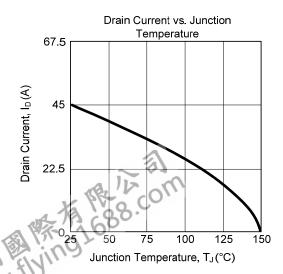




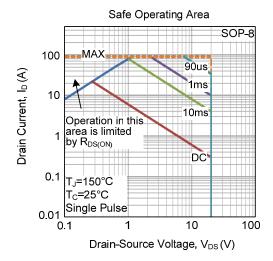








## ■ TYPICAL CHARACTERISTICS (Cont.)



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