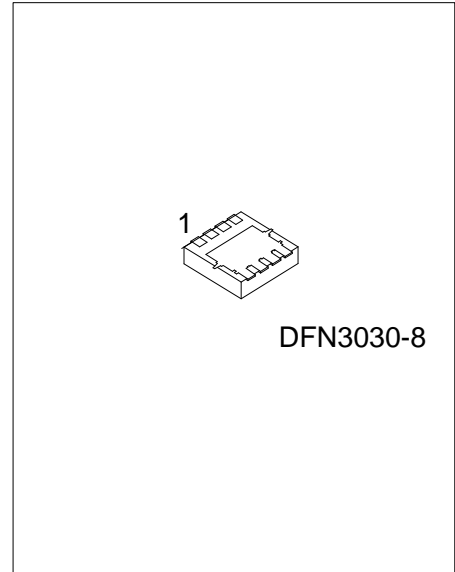




30V, 24A N-CHANNEL ENHANCEMENT MODE POWER MOSFET



DESCRIPTION

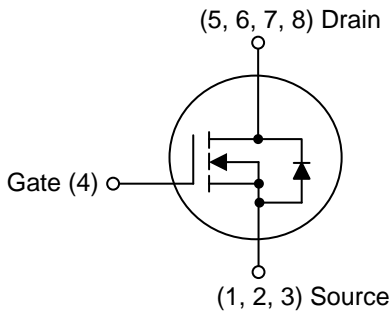
The UTC **UT7410** is an N-channel enhancement MOSFET, it uses UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$ and low gate charge.

The UTC **UT7410** is suitable for Load Switch and DC-DC converters applications, etc.

FEATURES

- * $R_{DS(ON)} \leq 17 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=8.0\text{A}$
- $R_{DS(ON)} \leq 26 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=7.0\text{A}$

SYMBOL



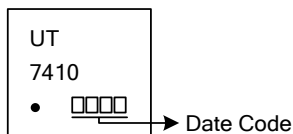
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing		
Lead Free	Halogen Free		1	2	3	4	5	6		7	8
UT7410L-K08-3030-R	UT7410G-K08-3030-R	DFN3030-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT7410G-K08-3030-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) K08-3030: DFN3030-8</p> <p>(3) G: Halogen Free and Lead Free, K: Lead Free</p>
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MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous (Note 2) $T_C=25^\circ\text{C}$	I_D	24	A
	Pulsed (Note 3)	I_{DM}	40	A
Power Dissipation (Note 2) $T_C=25^\circ\text{C}$		P_D	20	W
Junction Temperature		T_J	$-55 \sim +150$	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1)	Steady-State	θ_{JA}	60	$^\circ\text{C/W}$
Junction to Case (Note 2)	Steady-State	θ_{JC}	6.25	$^\circ\text{C/W}$

- Notes: 1. The value of θ_{JA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $\theta_{JA} t \leq 10\text{s}$ value and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
2. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

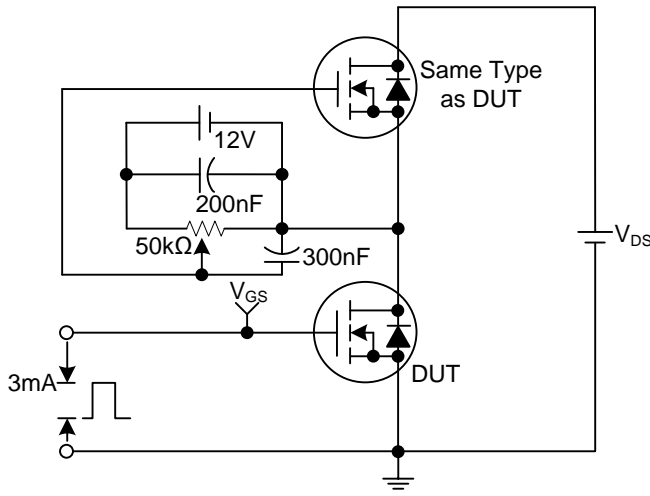
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	30			V	
Drain-Source Leakage Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA	
Gate-Source Leakage Current	Forward	I _{GSS} V _{GS} =+20V, V _{DS} =0V V _{GS} =-20V, V _{DS} =0V			+100	nA	
	Reverse				-100	nA	
ON CHARACTERISTICS							
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.4	1.8	2.5	V	
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =8.0A		13	17	mΩ	
		V _{GS} =4.5V, I _D =7.0A		22	26	mΩ	
On State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =5V	40			A	
DYNAMIC PARAMETERS							
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =15V, f=1.0MHz		421		pF	
Output Capacitance	C _{OSS}			110		pF	
Reverse Transfer Capacitance	C _{RSS}			92		pF	
Gate resistance	R _G	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		4	4.9	Ω	
SWITCHING PARAMETERS							
Total Gate Charge	10V	Q _G	V _{GS} =10V, V _{DS} =15V, I _D =20A		13		nC
	4.5V				7		nC
Gate to Source Charge	Q _{GS}			1.8		nC	
Gate to Drain Charge	Q _{GD}			3		nC	
Turn-ON Delay Time	t _{D(ON)}	V _{GS} =10V, V _{DS} =15V, I _D =20A, R _{GEN} =3Ω			5		ns
Rise Time	t _R				14		ns
Turn-OFF Delay Time	t _{D(OFF)}			13		ns	
Fall-Time	t _F			22		ns	
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current	I _S				1.7	A	
Drain-Source Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V		0.75	1	V	

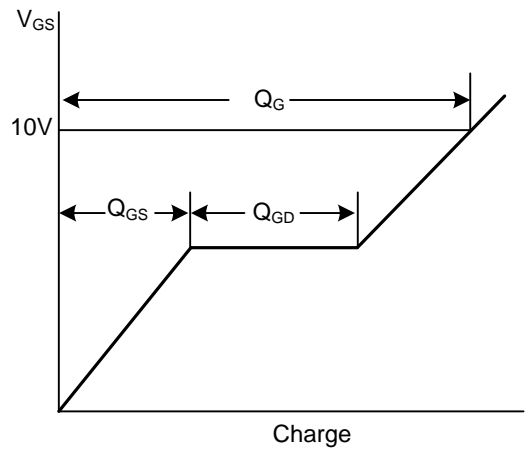
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating ambient temperature.

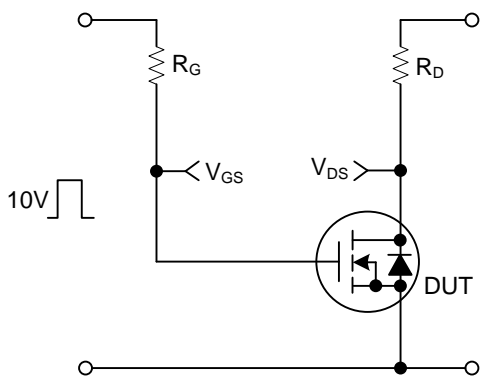
■ TEST CIRCUITS AND WAVEFORMS



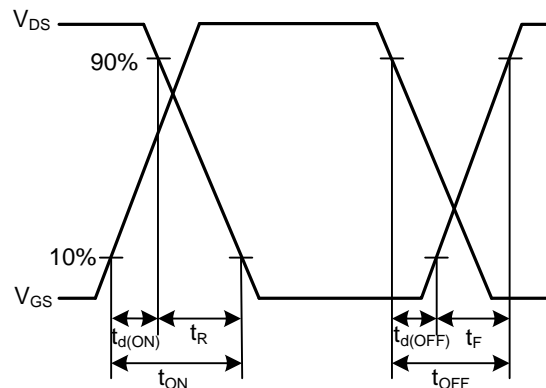
Gate Charge Test Circuit



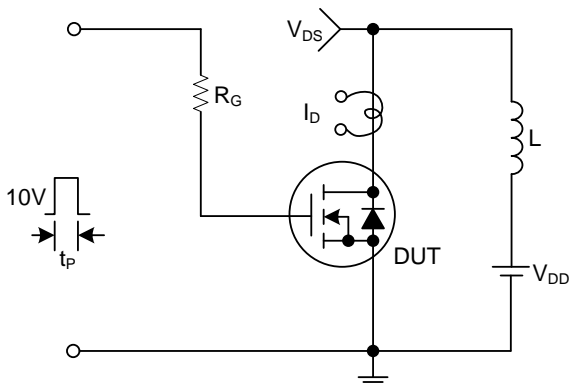
Gate Charge Waveforms



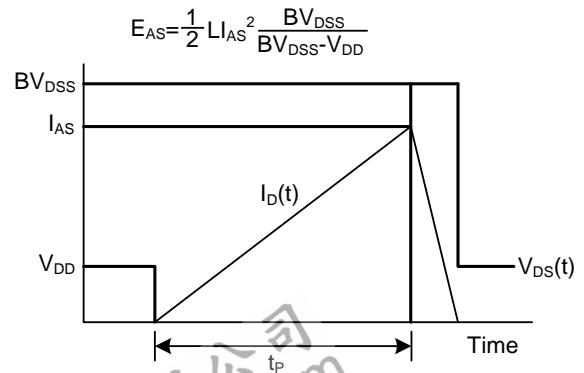
Resistive Switching Test Circuit



Resistive Switching Waveforms



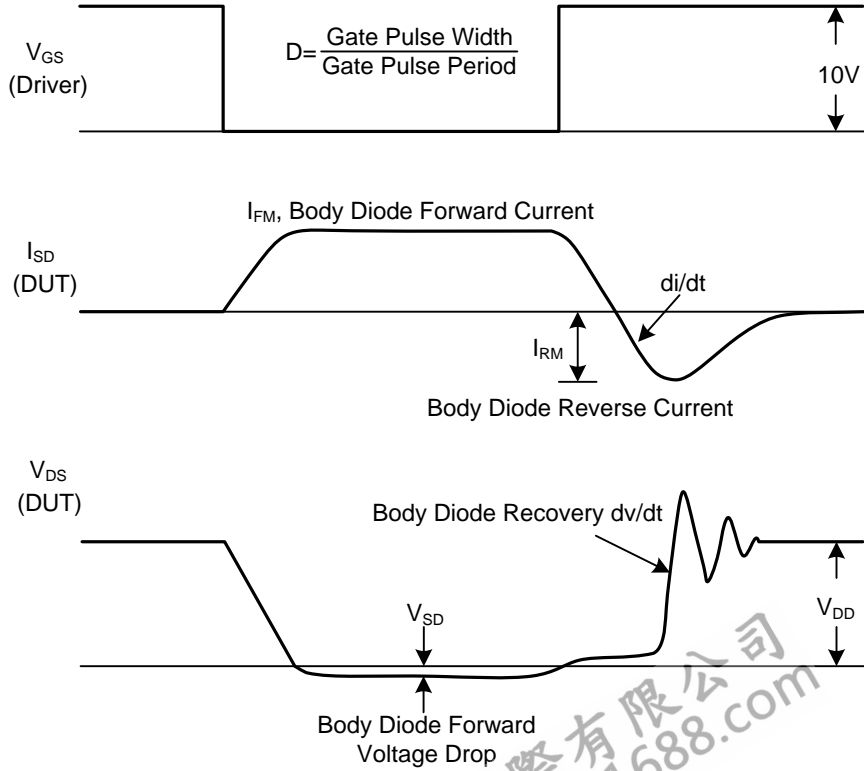
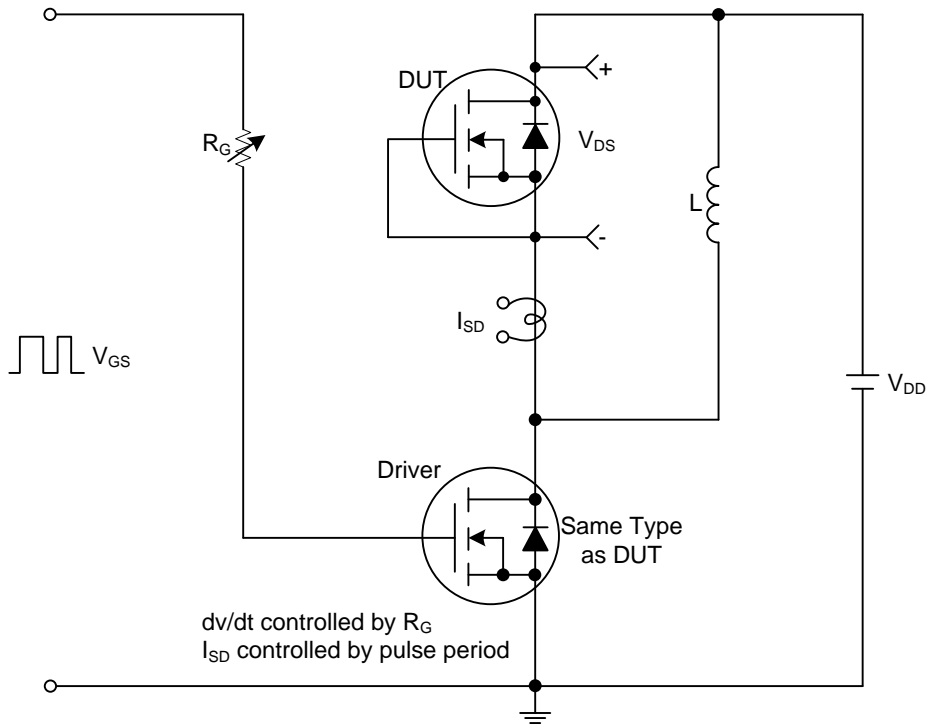
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit and Waveforms

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