



UTT4N10

Power MOSFET

3.5A, 100V N-CHANNEL TRENCHMOS LOGIC LEVEL FET

DESCRIPTION

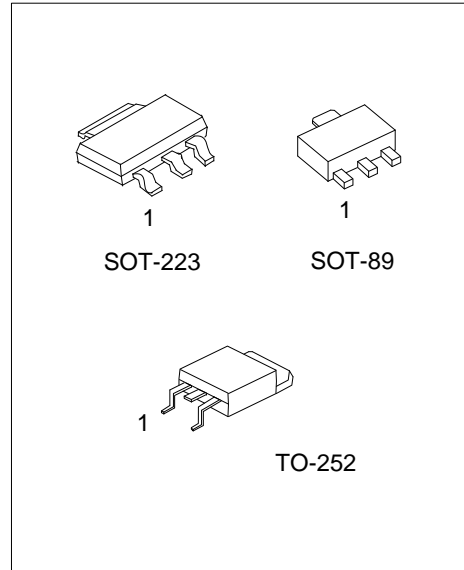
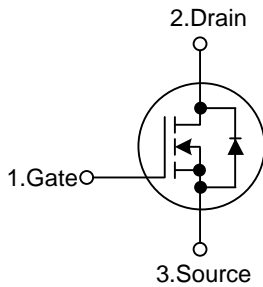
The UTC **UTT4N10** is an N-Channel Trench MOS Logic Level FET, it uses UTC's advanced technology to provide customers with a minimum on-state resistance and low gate charge.

The UTC **UTT4N10** is suitable for consumer, computing and communications, etc.

FEATURES

* $R_{DS(ON)} \leq 250 \text{ m}\Omega$ @ $V_{GS}=5\text{V}$, $I_D=1.75\text{A}$

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT4N10L-AA3-R	UTT4N10G-AA3-R	SOT-223	G	D	S	Tape Reel
UTT4N10L-AB3-R	UTT4N10G-AB3-R	SOT-89	G	D	S	Tape Reel
UTT4N10L-TN3-R	UTT4N10G-TN3-R	TO-252	G	D	S	Tape Reel

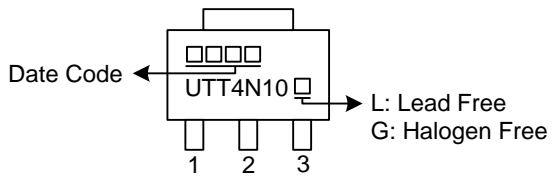
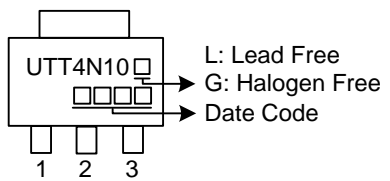
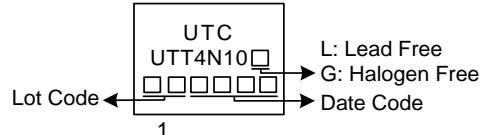
Note: Pin Assignment: G: Gate D: Drain S: Source

UTT4N10G-AA3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AA3: SOT-223, AB3: SOT-89, TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

PACKAGE	MARKING
SOT-89	 <p>The diagram shows a SOT-89 package with three leads labeled 1, 2, and 3. The marking area contains the text "UTT4N10" and three small squares. An arrow labeled "Date Code" points to the three squares. To the right, an arrow points to the text "L: Lead Free" and "G: Halogen Free".</p>
SOT-223	 <p>The diagram shows a SOT-223 package with three leads labeled 1, 2, and 3. The marking area contains the text "UTT4N10" and three small squares. An arrow labeled "Date Code" points to the three squares. To the right, an arrow points to the text "L: Lead Free" and "G: Halogen Free".</p>
TO-252	 <p>The diagram shows a TO-252 package with one lead labeled 1. The marking area contains the text "UTC" above "UTT4N10" and five small squares. An arrow labeled "Lot Code" points to the five squares. To the right, an arrow points to the text "L: Lead Free" and "G: Halogen Free". Another arrow points to the text "Date Code".</p>

■ **ABSOLUTE MAXIMUM RATINGS** ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage	$T_J \geq 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$	V_{DSS}	100	V	
Drain-Gate Voltage	$T_J \geq 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$, $R_{GS}=20\text{k}\Omega$	V_{DGR}	100	V	
Gate-Source Voltage		V_{GSS}	± 16	V	
Drain Current	Continuous	I_D	$T_C=100^\circ\text{C}$, $V_{GS}=5\text{V}$	2.2	A
			$T_C=25^\circ\text{C}$, $V_{GS}=5\text{V}$	3.5	A
	Pulsed	I_{DM}	$T_C=25^\circ\text{C}$, $t_p \leq 10\mu\text{s}$	14	A
Non-Repetitive Avalanche Current	$V_{GS}=5\text{V}$, $V_{DD} \leq 15\text{V}$, $R_{GS}=50\Omega$, Unclamped	I_{AS}	3.5	A	
Non-Repetitive Avalanche Energy	$V_{GS}=5\text{V}$, $V_{DD} \leq 15\text{V}$, $R_{GS}=50\Omega$, $I_D=3.5\text{A}$, Unclamped, $t_p=0.2\text{ms}$	E_{AR}	45	mJ	
Power Dissipation	SOT-223	P_D	6	W	
	SOT-89		3.5	W	
	TO-252		32	W	
Junction Temperature		T_J	-65 ~ +150	$^\circ\text{C}$	
Storage Temperature Range		T_{STG}	-65 ~ +150	$^\circ\text{C}$	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **THERMAL DATA (NOTE)**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-223	θ_{JA}	140	$^\circ\text{C/W}$
	SOT-89		180	$^\circ\text{C/W}$
	TO-252		80	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

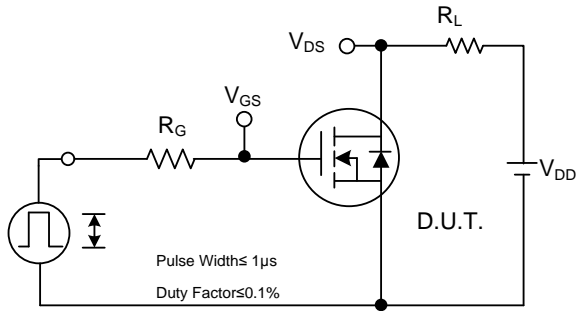
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V, T _J =-55°C	89			V
		I _D =250μA, V _{GS} =0V, T _J =25°C	100	130		V
Gate-Source Leakage Current	I _{GSS}	V _{GS} =+10V, V _{DS} =0V, T _J =25°C		10	100	nA
		V _{GS} =-10V, V _{DS} =0V, T _J =25°C		-10	-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA, T _J =25°C	1		3	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =5V, I _D =1.75A, T _J =25°C		200	250	mΩ
		V _{GS} =5V, I _D =1.75A, T _J =150°C			575	mΩ
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{GS} =10V, V _{DS} =50V, I _D =1.3A, T _J =25°C		20		nC
Gate to Source Charge	Q _{GS}			3.7		nC
Gate to Drain Charge	Q _{GD}			3.6		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DS} =50V, V _{GS} =10V, R _L =0.5Ω, R _{G(ext)} =6Ω, T _J =25°C		30		ns
Rise Time	t _R			30		ns
Turn-OFF Delay Time	t _{D(OFF)}			140		ns
Fall-Time	t _F			30		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S	T _J =25°C			3.5	A
Maximum Body-Diode Pulsed Current	I _{SM}	T _J =25°C, t _p ≤10μs			14	A
Drain-Source Diode Forward Voltage	V _{SD}	I _S =3.5A, V _{GS} =0V, T _J =25°C		0.87	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	I _S =3.5A, V _{GS} =0V, di _S /dt=-100A/μs,		50		ns
Body Diode Reverse Recovery Charge	Q _{rr}	V _{DS} =30V, T _J =25°C		100		nC

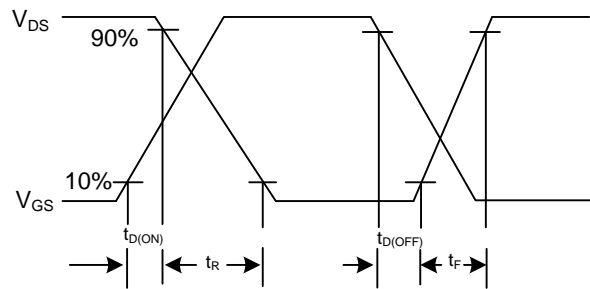
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating ambient temperature.

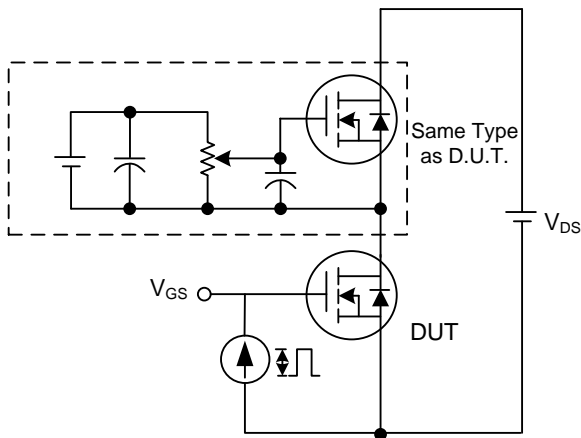
TEST CIRCUITS AND WAVEFORMS



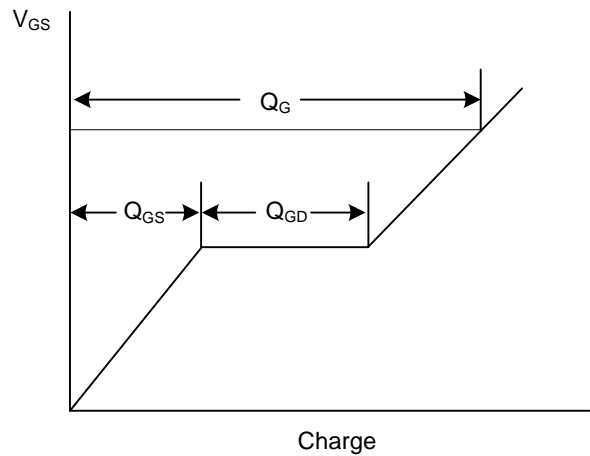
Switching Test Circuit



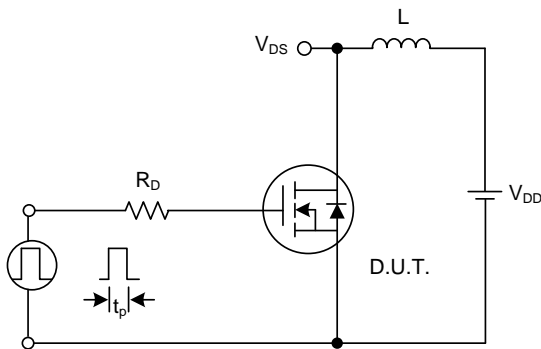
Switching Waveforms



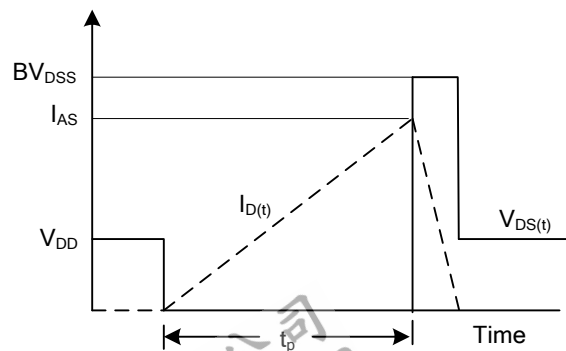
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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