

UNISONIC TECHNOLOGIES CO., LTD

UTT75N07

Preliminary

75A, 70V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

DESCRIPTION

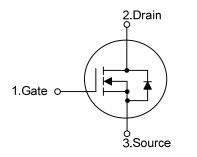
The UTC **UTT75N07** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ and high switching speed characteristic by high cell density trench and low gate charge technology.

The UTC **UTT75N07** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

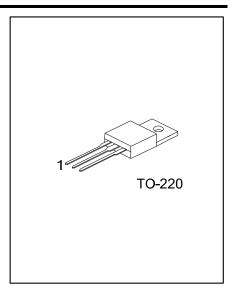
- * $R_{DS(ON)} \le 10 \text{ m}\Omega$ @ V_{GS} =10V, I_D =37.5A
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL



ORDERING INFORMATION

| Ordering Number | | Daakaga | Pin Assignment | | | Deaking | |
|------------------------------------------------------------------------------------|----------------------------------------------------|---------|----------------|---------------|----------|---------|--|
| Lead Free Halogen Free | | Package | 1 | 2 | 3 | Packing | |
| UTT75N07L-TA3-T | UTT75N07L-TA3-T UTT75N07G-TA3-T | | G | D | S | Tube | |
| Note: Pin Assignment: G: 0 | Gate D: Drain S: Source | | | | | | |
| | (1) T: Tube (2) TA3: TO-22((3) L: Lead Free | | ogen Fre | e and Le | ead Free | | |
| ■ MARKING UTC UTT 75N07 L: Lead Free G: Halogen Free Data Code 1 | | | | | | | |
| www.unisonic.com.tw | | | | | | 1 of 5 | |
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■ **ABSOLUTE MAXIMUM RATING** (T_c=25°C, unless otherwise specified)

| PARAMETER | | SYMBOL | RATINGS | UNIT | |
|------------------------------------|------------------------|------------------|------------|------|--|
| | | | | UNIT | |
| Drain-Source Voltage | | V _{DSS} | 70 | V | |
| Gate-Source Voltage | | V _{GSS} | ±20 | V | |
| Drain Current | Continuous | Ι _D | 75 | А | |
| | Pulsed (Note 2) | I _{DM} | 300 | А | |
| Avalanche Energy | Single Pulsed (Note 3) | E _{AS} | 1382 | mJ | |
| Peak Diode Recovery dv/dt (Note 4) | | dv/dt | 13 | V/ns | |
| Power Dissipation | | PD | 110 | W | |
| Junction Temperature | | TJ | +150 | °C | |
| Storage Temperature Range | | T _{STG} | -55 ~ +150 | °C | |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3. L = 120mH, I_{AS} = 4.8A, V_{DD} = 48V, R_G = 25 Ω , Starting T_J = 25°C.
- 4. $I_{SD} \leq 30A$, di/dt $\leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^{\circ}C$.

THERMAL RESISTANCES CHARACTERISTICS

| PARAMETER | SYMBOL | RATINGS | UNIT | |
|---------------------|-----------------|---------|------|--|
| Junction to Ambient | θ _{JA} | 62 | °C/W | |
| Junction to Case | θ _{JC} | 1.13 | °C/W | |

■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

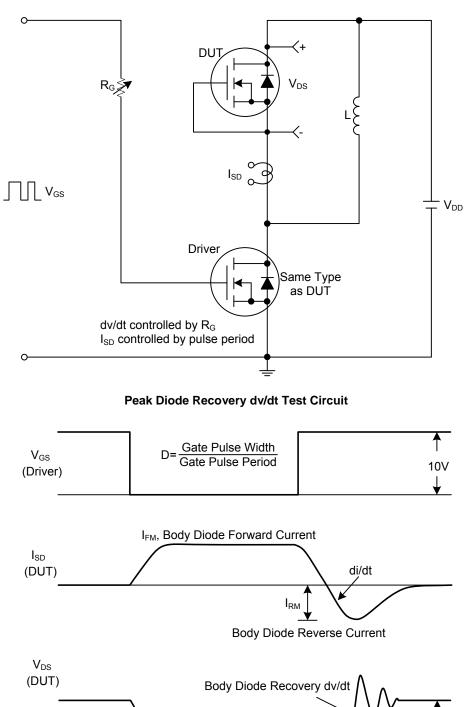
| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------------|--------------|---------------------|--------------------------------------------------------------------------------------------------------|-----|------|------|------|
| OFF CHARACTERISTICS | | | | | | | |
| Drain-Source Breakdown Voltage | | BV _{DSS} | I _D =250μA, V _{GS} =0V | 70 | | | V |
| Drain-Source Leakage Current | | I _{DSS} | V _{DS} =70V, V _{GS} =0V | | | 1.0 | μA |
| Gate-Source Leakage Current | Forward | 1 | V _{GS} =+20V, V _{DS} =0V | | | +100 | nA |
| | Reverse | I _{GSS} | V _{GS} =-20V, V _{DS} =0V | | | -100 | nA |
| ON CHARACTERISTICS | | | | | | | |
| Gate Threshold Voltage | | V _{GS(TH)} | V _{DS} =V _{GS} , I _D =250µA | | | 3.0 | V |
| Static Drain-Source On-State Resistance | | R _{DS(ON)} | V _{GS} =10V, I _D =37.5A | | | 10 | mΩ |
| DYNAMIC PARAMETERS | | | | | | | |
| Input Capacitance | | CISS | | | 3700 | | pF |
| Output Capacitance | | Coss | V _{GS} =0V, V _{DS} =25V, f=1.0MHz | | 290 | | pF |
| Reverse Transfer Capacitance | | C _{RSS} | | | 245 | | pF |
| SWITCHING PARAMETERS | | | | | | | |
| Total Gate Charge (Note 1) | | Q_{G} | | | 430 | | nC |
| Gate to Source Charge | | Q_{GS} | V _{DS} =50V, V _{GS} =10V, I _D =1.3A, I _G =100µA (Note 1, 2) | | 20 | | nC |
| Gate to Drain Charge | | Q_{GD} | | | 34 | | nC |
| Turn-on Delay Time (Note 1) | | t _{D(ON)} | | | 64 | | ns |
| Rise Time | | t _R | V _{DD} =30V, V _{GS} =10V, I _D =0.5A, | | 120 | | ns |
| Turn-off Delay Time | | t _{D(OFF)} | R _G =25Ω (Note 1, 2) | | 1700 | | ns |
| Fall-Time | | t _F | | | 420 | | ns |
| SOURCE- DRAIN DIODE RATIN | GS AND CH | ARACTERIS | TICS | | | | |
| Maximum Body-Diode Continuous Current | | Is | ~~~~~ | | | 75 | Α |
| Maximum Body-Diode Pulsed Current | | I _{SM} | TRE CON | | | 300 | Α |
| Drain-Source Diode Forward Voltage (Note 1) | | V_{SD} | I _S =75A, V _{GS} =0V | | | 1.2 | V |
| Reverse Recovery Time (Note 1) | | t _{rr} | I _S =30A, V _{GS} =0V, | | 66 | | nS |
| Reverse Recovery Charge | | Qrr | dl _F /dt =100A/µs | | 0.1 | | μC |
| Notes: 1. Pulse Test : Pulse width | n < 300us Du | ty cycle $\leq 2\%$ | | | | | |

Notes: 1. Pulse Test : Pulse width \leq 300µs, Duty cycle \leq 2%.

2. Essentially independent of operating ambient temperature.



■ TEST CIRCUITS AND WAVEFORMS



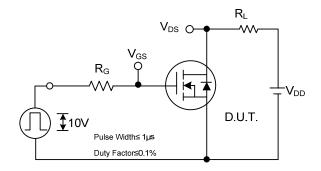
SD

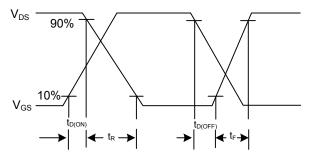
Body Diode Forward Voltage Drop Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

 V_{DD}

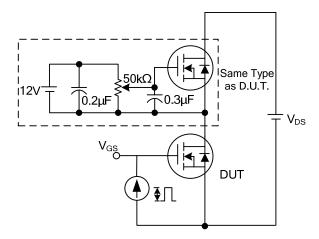
TEST CIRCUITS AND WAVEFORMS



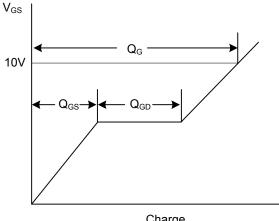


Switching Test Circuit



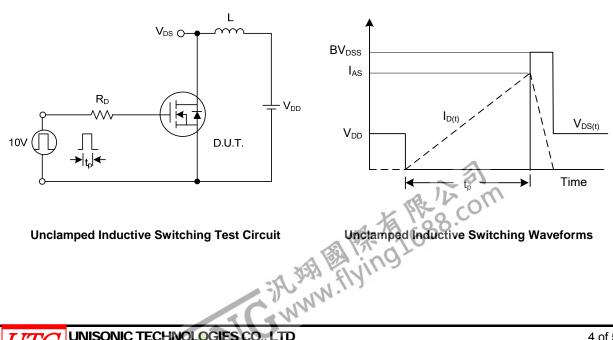


Gate Charge Test Circuit



Charge





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