



UTT75P03

Preliminary

Power MOSFET

-75A, -30V P-CHANNEL POWER MOSFET

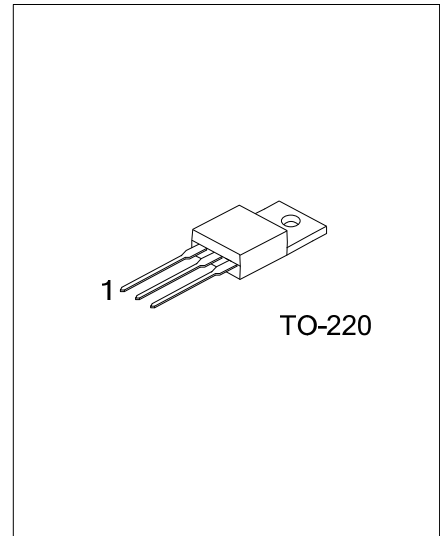
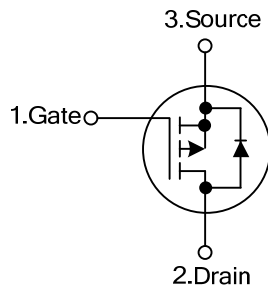
DESCRIPTION

The UTC **UTT75P03** is a P-channel power MOSFET using UTC's advanced technology to provide the customers with high switching speed, high current capacity and a minimum on-state resistance.

FEATURES

- * $R_{DS(ON)} < 7.0m\Omega @ V_{GS}=-10V, I_D=-30A$
- * High Switching Speed
- * High Current Capacity

SYMBOL



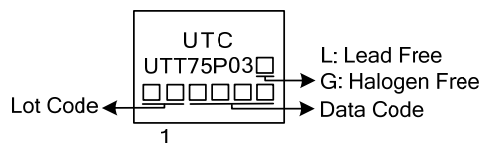
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT75P03L-TA3-T	UTT75P03G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT75P03L-TA3-T 	(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V_{DSS}	-30	V	
Gate-Source Voltage		V_{GSS}	± 20	V	
Drain Current	Continuous	I_D	$T_C=25^{\circ}\text{C}$	-75 (Note 2)	A
			$T_C=125^{\circ}\text{C}$	-65	A
	Pulsed	I_{DM}	-240	A	
Avalanche Current		I_{AR}	-60	A	
Repetitive Avalanche Energy (Note 3)		$L=0.1\text{mH}$	E_{AR}	180	mJ
Power Dissipation		$T_C=25^{\circ}\text{C}$	P_D	187	W
Junction Temperature		T_J	-55 ~ +175	$^{\circ}\text{C}$	
Storage Temperature		T_{STG}	-55 ~ +175	$^{\circ}\text{C}$	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Package limited.

3. Duty cycle $\leq 1\%$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.8	$^{\circ}\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

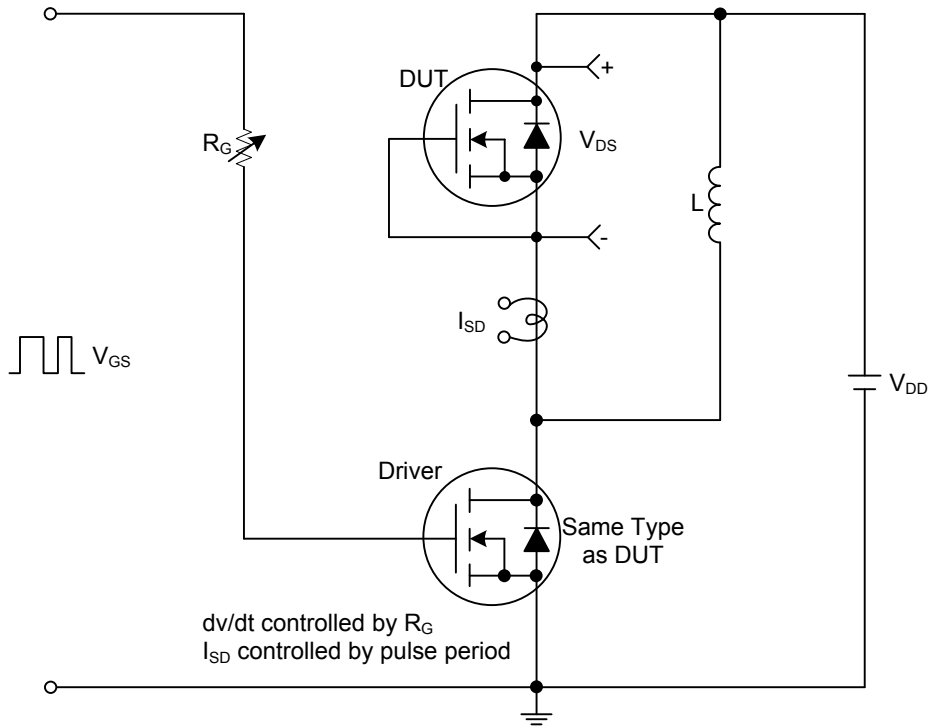
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$			-50	μA
		$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$, $T_J=175^\circ\text{C}$			-250	μA
Gate- Source Leakage Current	Forward	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1		-3	V
Static Drain-Source On-State Resistance (Note 1)	$R_{DS(ON)}$	$V_{GS}=-10\text{V}$, $I_D=-30\text{A}$		5.5	7	m Ω
		$V_{GS}=-10\text{V}$, $I_D=-30\text{A}$, $T_J=125^\circ\text{C}$			10	m Ω
		$V_{GS}=-10\text{V}$, $I_D=-30\text{A}$, $T_J=175^\circ\text{C}$			13	m Ω
		$V_{GS}=-4.5\text{V}$, $I_D=-20\text{A}$		8	10	m Ω
On State Drain Current (Note 1)	$I_{D(ON)}$	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-120			A
DYNAMIC PARAMETERS (Note 2)						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=-25\text{V}$, $f=1.0\text{MHz}$		9000		pF
Output Capacitance	C_{OSS}			1565		pF
Reverse Transfer Capacitance	C_{RSS}			715		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-75\text{A}$ (Note 3)		160	240	nC
Gate to Source Charge	Q_{GS}			32		nC
Gate to Drain Charge	Q_{GD}			30		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=-15\text{V}$, $R_L=0.2\Omega$, $I_D\approx-75\text{A}$, $V_{GEN}=-10\text{V}$, $R_G=2.5\Omega$ (Note 3)		25	40	ns
Rise Time	t_R			225	360	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			150	240	ns
Fall-Time	t_F			210	340	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C=25^\circ\text{C}$) (Note 2)						
Maximum Body-Diode Continuous Current	I_S				-75	A
Maximum Body-Diode Pulsed Current	I_{SM}				-240	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_F=-75\text{A}$, $V_{GS}=0\text{V}$		-1.2	-1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F=-75\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		55	100	ns
Body Diode Reverse Recovery Charge	Q_{rr}			0.07	0.25	μC
Peak Reverse Recovery Current	$I_{RM(REC)}$			2.5	5	A

Notes: 1. Pulse test; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

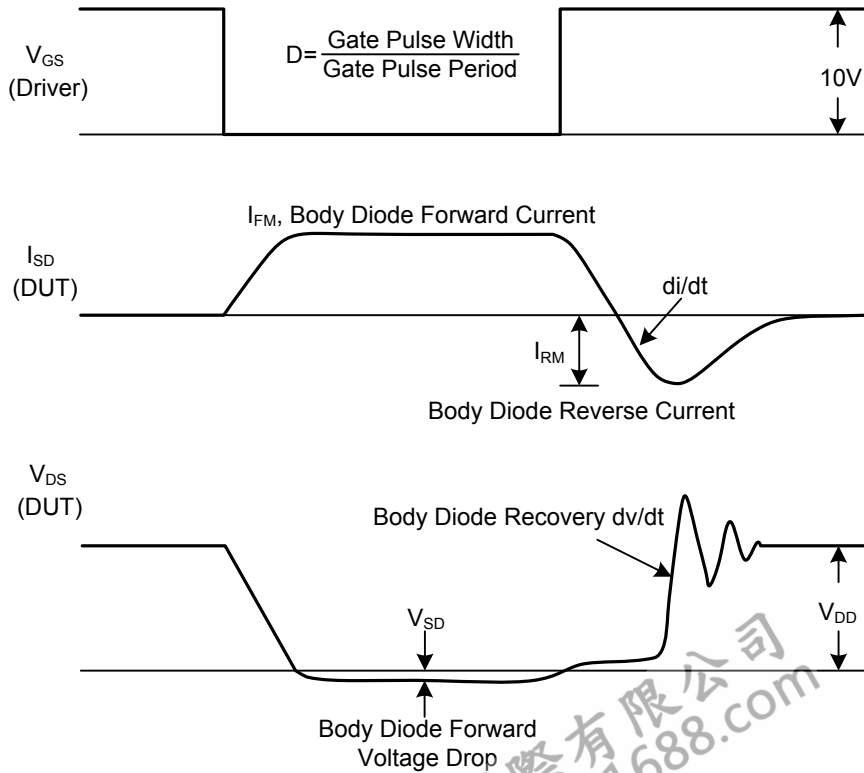
2. Guaranteed by design, not subject to production testing.

3. Independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



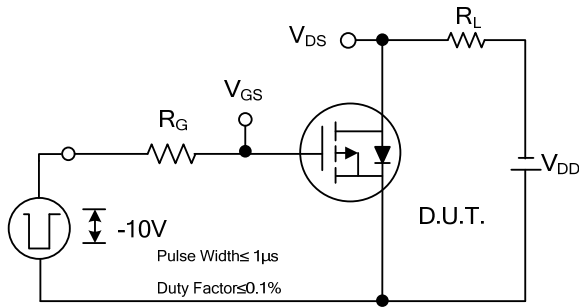
Peak Diode Recovery dv/dt Test Circuit



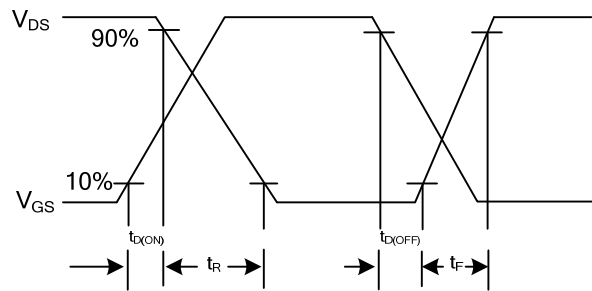
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

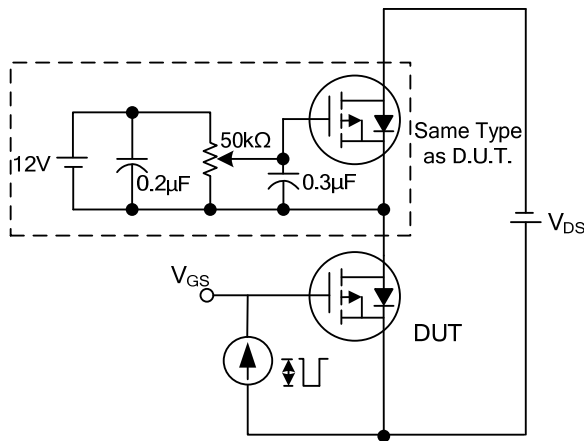
TEST CIRCUITS AND WAVEFORMS



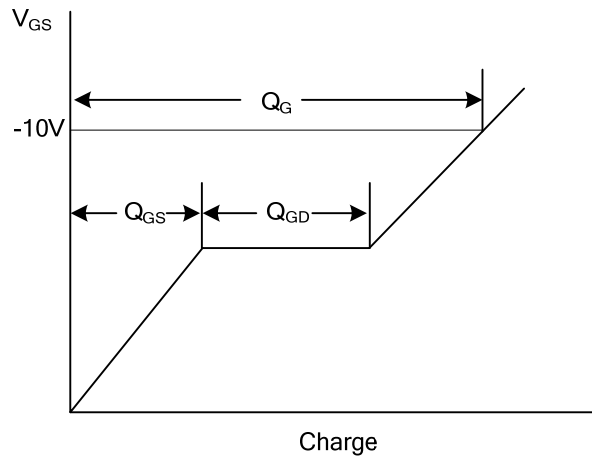
Switching Test Circuit



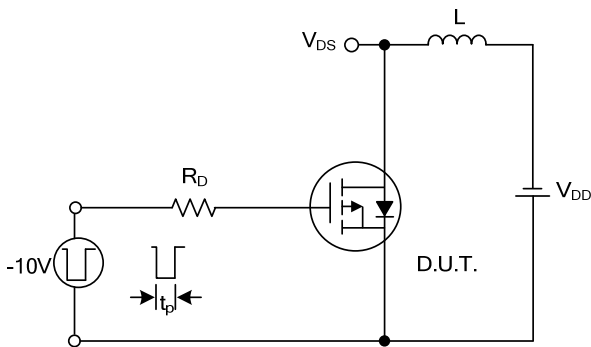
Switching Waveforms



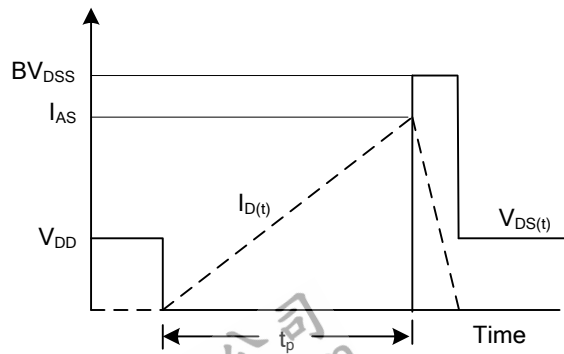
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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