



UTT85N15

Preliminary

POWER MOSFET

85A, 150V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

DESCRIPTION

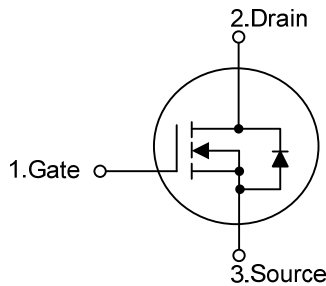
The UTC **UTT85N15** is an N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low voltage inverter applications.

The UTC **UTT85N15** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

- * $R_{DS(ON)} < 18.5m\Omega @ V_{GS}=10V, I_D=40A$
- $R_{DS(ON)} < 24m\Omega @ V_{GS}=4.5V, I_D=20A$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL

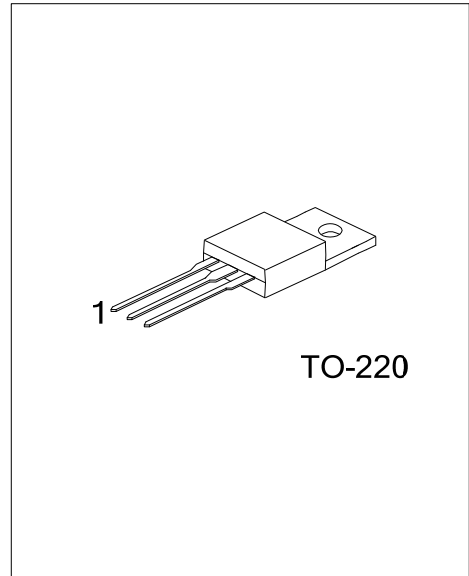


ORDERING INFORMATION

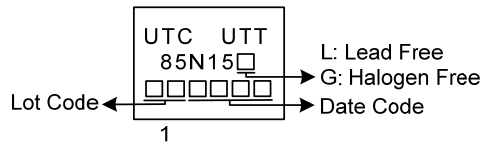
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT85N15L-TA3-T	UTT85N15G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT85N15G-TA3-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) TA3: TO-220
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



MARKING



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■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	150	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	85	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	120	A
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.2	V/nS
Power Dissipation		P_D	100	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $I_{SD} \leq 30\text{A}$, $di/dt \leq 50\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^\circ\text{C}$.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	1.25	$^\circ\text{C}/\text{W}$

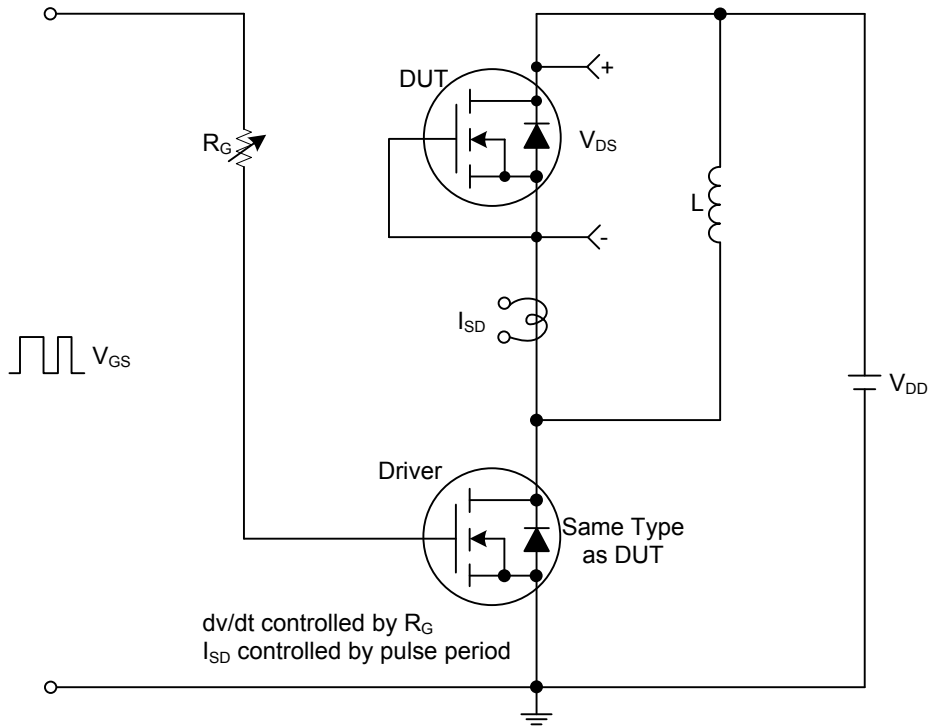
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	150			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=120\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	I_{GSS}	Forward			+100	nA
		Reverse	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			-100
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=40\text{A}$			18.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$			24	$\text{m}\Omega$
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		10000		pF
Output Capacitance	C_{OSS}			485		pF
Reverse Transfer Capacitance	C_{RSS}			340		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$, $I_D=1\text{mA}$ (Note 1, 2)		390		nC
Gate to Source Charge	Q_{GS}			40		nC
Gate to Drain Charge	Q_{GD}			44		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		53		ns
Rise Time	t_R			60		ns
Turn-off Delay Time	$t_{D(OFF)}$			930		ns
Fall-Time	t_F			340		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				85	A
Maximum Body-Diode Pulsed Current	I_{SM}				120	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=85\text{A}$, $V_{GS}=0\text{V}$			2.0	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S=30\text{A}$, $V_{GS}=0\text{V}$		130		nS
Reverse Recovery Charge	Q_{rr}	$dI_F/dt=50\text{A}/\mu\text{s}$		300		nC

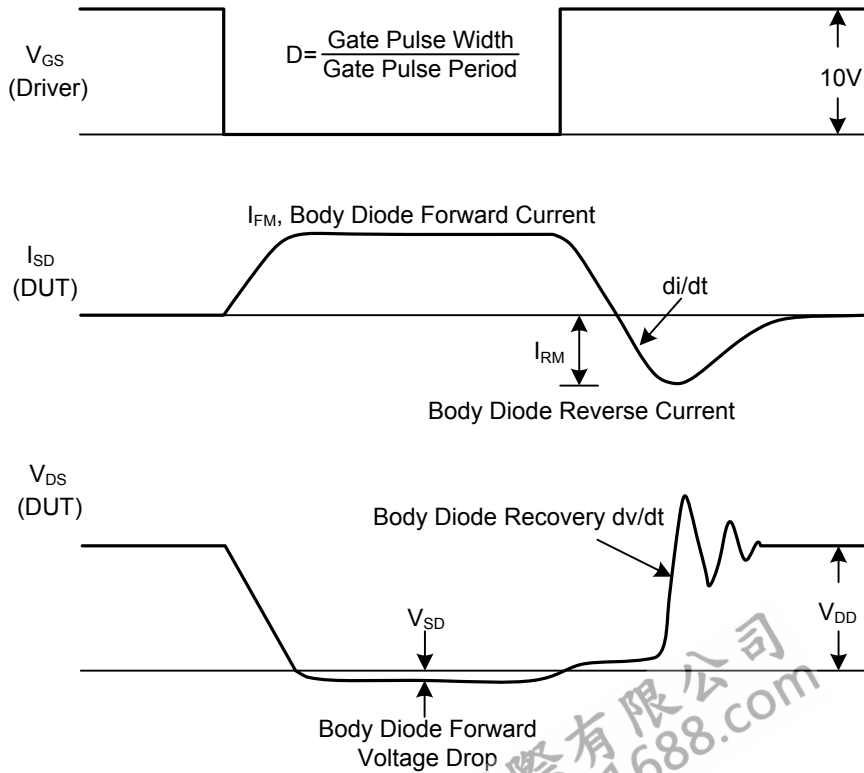
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

TEST CIRCUITS AND WAVEFORMS



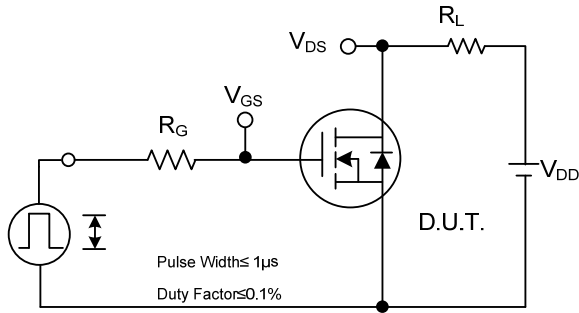
Peak Diode Recovery dv/dt Test Circuit



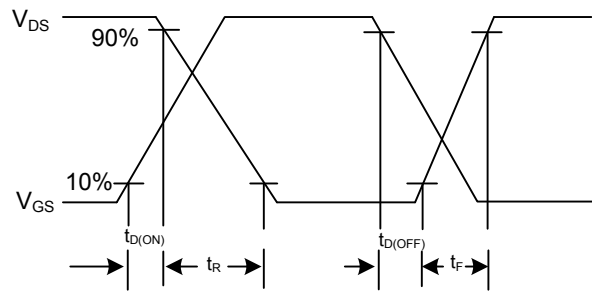
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

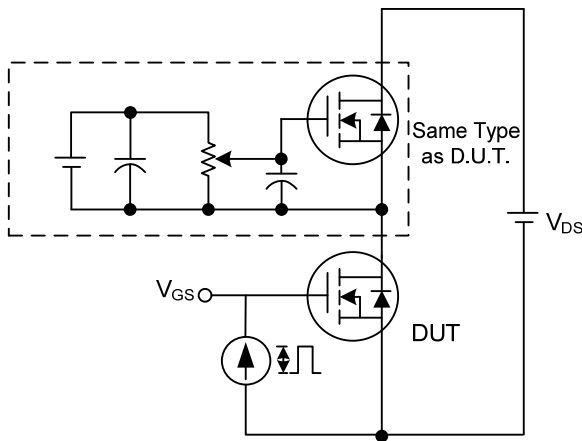
■ TEST CIRCUITS AND WAVEFORMS



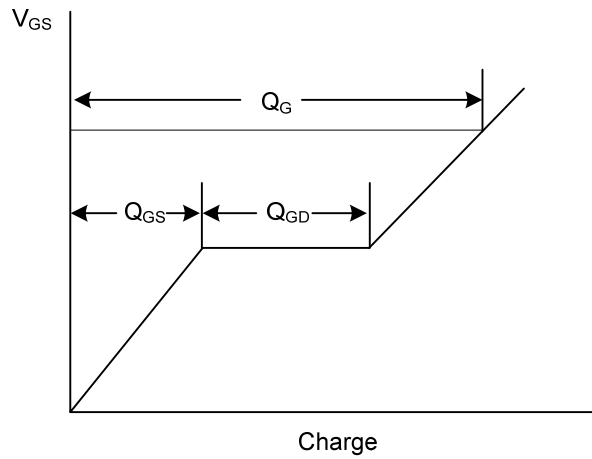
Switching Test Circuit



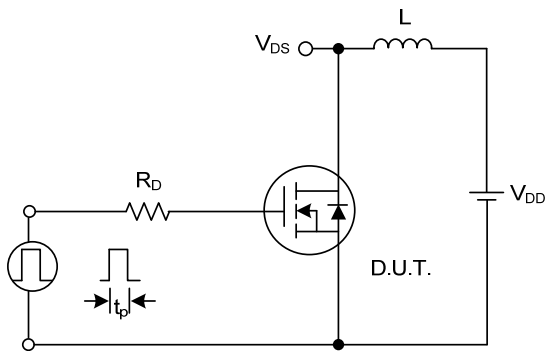
Switching Waveforms



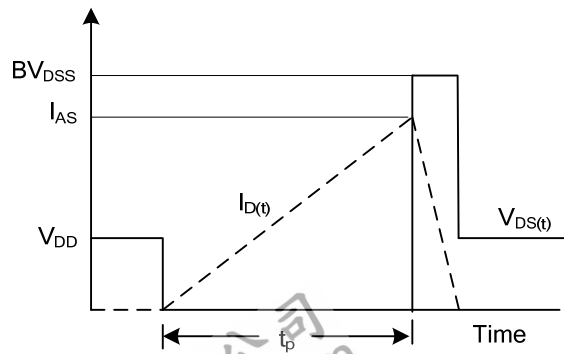
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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