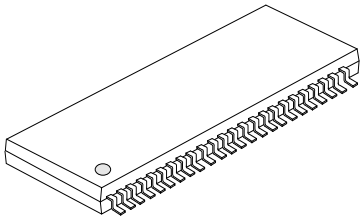
LCD SEGMENT DRIVERS
STANDARD SEGMENT DRIVER



TSSOP-48

■ DESCRIPTION

The UTC **UU97950** is a LCD Segment Drivers with I2C serial Interface (SCL, SDA). Inergrated RAM for display data:35×8bit and Electrial Volume register.

Typical applications of UTC **UU97950** are Telephone, FAX, portable equipments(POS,ESR…) DSC, DVC Meter equipment etc.

■ FEATURES

* LCD driver port: 8 Common output,35 Segment output
* 2wire serial interface (SCL, SDA)
* Integrated RAM for display data(DDRAM): 35×8bit
* Integrated Oscillation circuit
* Integrated Power supply circuit for LCD driving
  1/4 Bias 1/8 Duty
* Integrated Electrial volume register function
* Low power consumption design
* Operation power supply: 2.5 ~ 5.5V

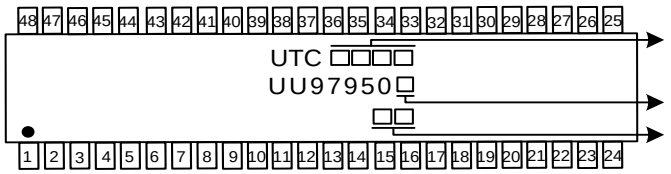
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UU97950L-P48-R	UU97950G-P48-R	TSSOP-48	Tape Reel

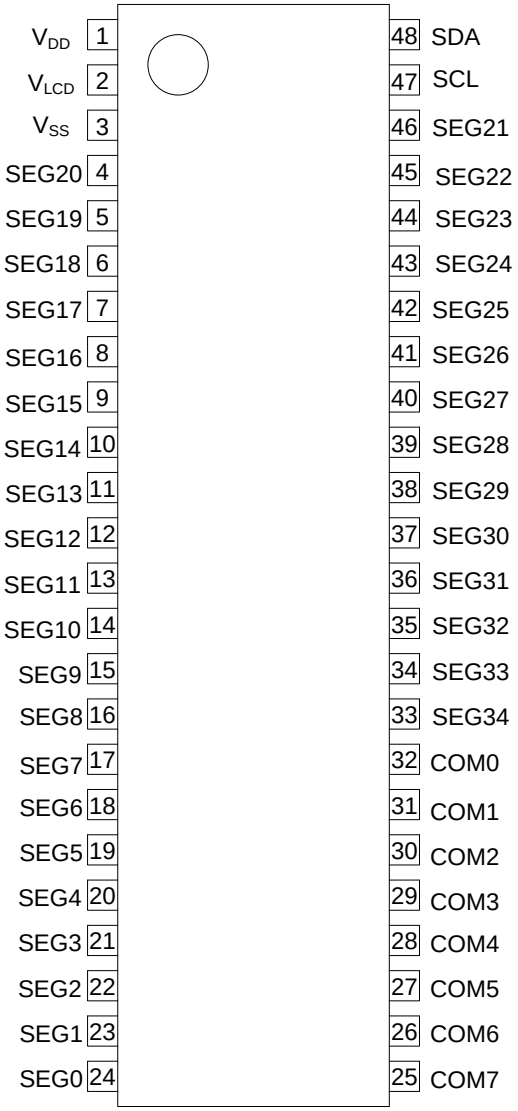
UU97950G-P48-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) P48: TSSOP-48
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



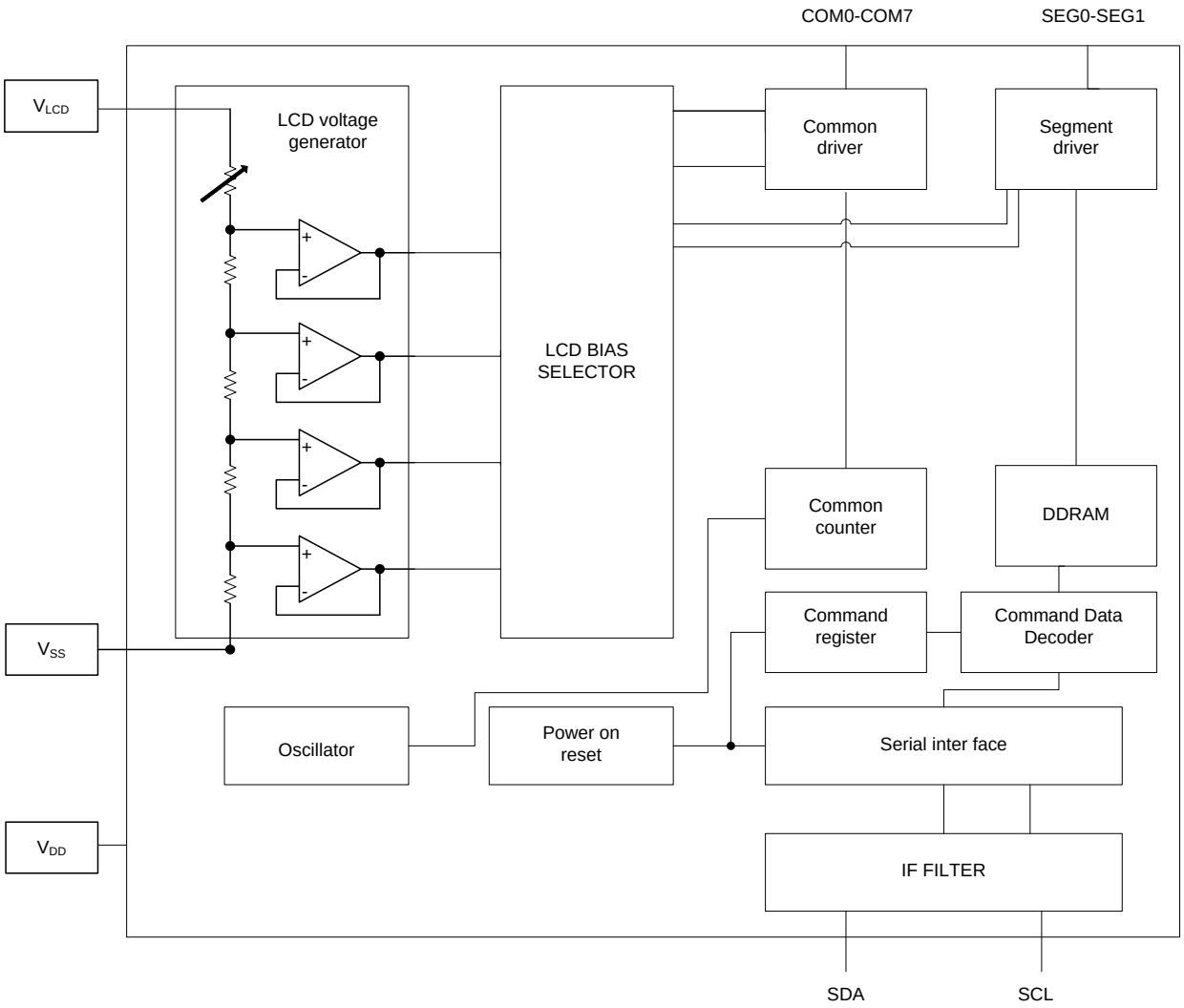
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{DD}	Power Supply
2	V_{LCD}	Power supply or LCD driving
3	V_{SS}	Supply GND reference.
4 ~ 24	SEG20-0	SEGMENT output or LCD driving
33 ~ 46	SEG34-21	
25 ~ 32	COM7-0	COMMON output for LCD driving
47	SCL	Serial data transfer clolk
48	SDA	Serial data input

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply	V_{DD}	-0.5 ~ +7	V
Power Supply for LCD driving	V_{LCD}	-0.5 ~ +7	V
Input voltage range	V_{IN}	-0.5 ~ V_{DD}+0.5	V
Operation temperature	T_{OPR}	-40 ~ +85	°C
Storage temperature range	T_{STG}	-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ STANDARD (RECOMMENDED) OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply	V_{DD}	2.5		5.5	V
Power Supply for LCD dirving	V_{LCD}	2.5		5.5	V
Operating Temperature Range	T_{OPR}	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

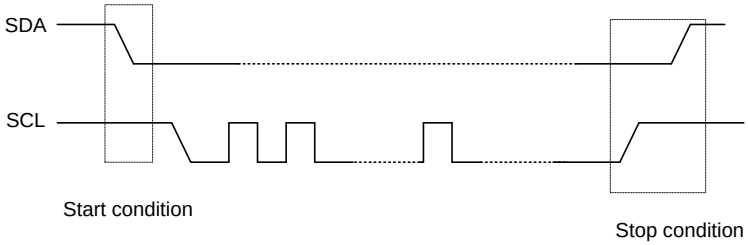
DC Characteristics (V_{DD}=2.5 ~ 5.5V, V_{LCD}=2.5 ~ 5.5V, V_{SS}=0V, T_A=-40 ~ 85°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
"H" level input voltage		V_{IH}	SDA SCL	0.7×V_{DD}		V_{DD}	V
"L" level input voltage		V_{IL}	SDA SCL	V_{SS}		0.3×V_{DD}	V
Standby current		I_{ST}	Display off Oscillation off			5	uA
Power consumption1		I_{DD}	V_{DD}=3.3V, V_{LCD}=5V, T_A=25°C, Power save mode1, FR=80Hz, 1/4 Bias, Frame inverse		2.5		uA
Power consumption2		I_{LCD}	V_{DD}=3.3V, V_{LCD}=5V, T_A=25°C, Power save mode1, FR=80Hz, 1/4 Bias, Frame inverse		10		uA
Frame frequency		f_{clk}	V_{DD}=3.3V		80		Hz
SCL cycle time		t_{scl}		2.5			us
LCD Driver on resistance	SEG	RON	I_{LOAD}=±10uA		3.5		KΩ
	COM				3.5		KΩ

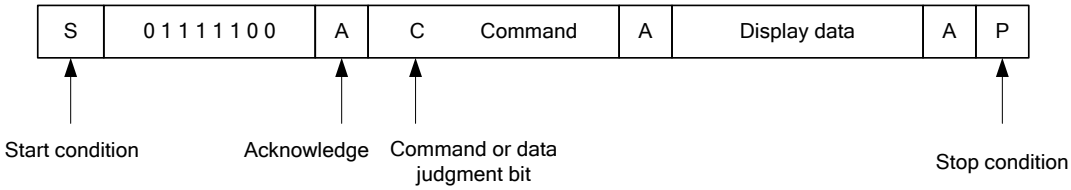
■ FUNCTION DESCRIPTIONS

Command /Data transfer method

This device is controlled by 2wire serial signal (SDA,SCL)



It has to generate the condition such as Start condition and Stop condition in 2 wire serial interface transfer method.



Method of how to transfer command and data is shown as follows.

1. Generate “start condition”
2. Issue Slave address
3. Transfer command and display data

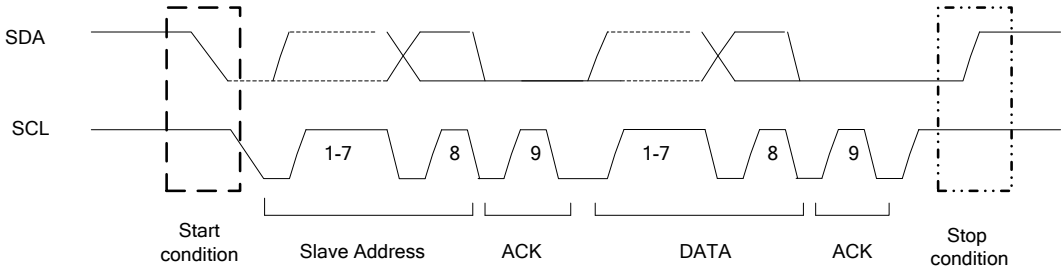
Acknowledge

Data format is 8bits and return Acknowledge after transfer 8bits data.

When SCL 8th=’L’ after transfer 8bit data (Slave Address, Command, Display Data), output open SDA line.

When SCL 9th=’L’ , stop output function.

If no need Acknowledge function, Please input ’L’ level from SCL 8th=’L’ to SCL 9th=’L’



■ FUNCTION DESCRIPTIONS (Cont.)

Command transfer method

Issue the Slave Address (01111100 for write mode or 01111101 for read mode) after the start condition is Generated. Command input follows after the Slave Address. The least significant bit (LSB) of the Slave Address determines if the operation to be done is Write or Read operation.

The MSB (command or data judgement bit) defines if the succeeding byte is a command or data.
When “Command or data judgement bit”=’1’, the next byte is a command.
When “Command or data judegment bit”=’0’, the nexit byte is display data.

S	Slave address	A	1 Command	A	1 Command	A	0 Command	A	Display	P

Once it enters display data transfer condition, it cannot input any command.
To input command again, please generate the “START condition” again.
If “START condition” or “STOP condition” is inputted in the middle of command transmission, the command will be cancelled. If the Slave address is continuously inputted following “START condition”, it will be in command input condition.

Please input “Slave Address” in the first data transmission after “START condition”.
When Slave Address cannot be recongnized in the first data transmission. Acknowledge does not return and the next transmission will be invalid. When data transmission is in invalid status and the “START condition” is transmitted again, it will return to valid status.

Write display and transfer method

Write mode happens when R/W bit=’0’
This device has Display Data RAM of 35×8=280bits.
The relationship between data input and display data, DDRAM data and address are as follows.

The 8-bit display data will be stored in the DDRAM. The address to be written is the address specified by Address Set command, and the address is automatically incremented after every 8-bits of data.
Data can be continuously written in the DDRAM by transmitting data continuously.

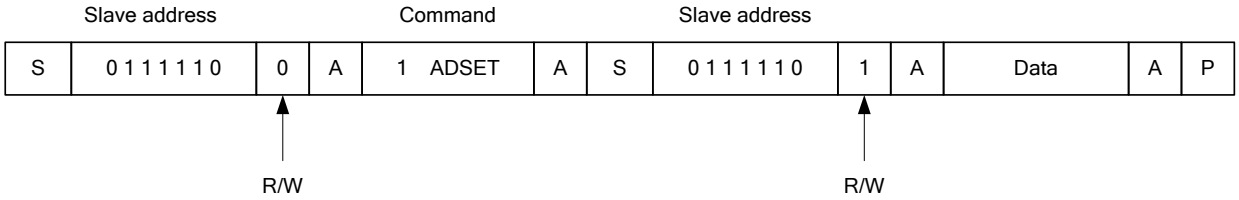
BIT	0	1	2	3	· · · · · · · · · · · · · · · · · · · ·	21h	22h	
0	a	i						COM0
1	b	j						COM1
2	c	k						COM2
3	d	l						COM3
4	e	m						COM4
5	f	n						COM5
6	g	o						COM6
7	h	p						COM7
	SEG0	SEG1	SEG2	SEG3		SEG33	SEG34	

DDRAM address

■ FUNCTION DESCRIPTIONS (Cont.)

Read Command Register and Transfer Method

The Command Registers can be read during read mode. The sequence for the command register read is shown below.



The command register addresses are described in 6. Command Description (ADSET command). The following register settings can be read in this mode.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	0	0	P5	P4	P3	P2	P1	P0	23h
REG2	P7	P6	P5	P4	P3	P2	P1	P0	24h

REG1: P5= Software reset condition
P4 to P0 = EVR setting
REG2: P7 to P6 = Frame Frequency (FR) setting
P5 to P4 = Power Save Mode (SR) setting
P3 = LCD drive waveform setting
P2 = Display ON/ OFF setting
P1= APON setting
P0 = APOFF setting

LCD Driver Bias Circuit

This device generates LCD driving voltage with on-chip Buffer AMP
And it can drive LCD at low power consumption.
Line and frame inversion set in DISCTL command.
Refer to the LCD driving waveform about each LCD diving waveform

Reset initialize condition

Initial condition after execute Software Reset is as follows.
Display OFF.
DDRAM address is initialized
Refer to Command Description about initialize value of register.

■ COMMAND / FUCTION LIST

Description List of Command / Function

	Command	Function
1	Address set(ADSET)	DDRAM address setting(00-22h)
2	EVR set (EVRSET)	EVR setting(0-31)
3	Display Control(DISCTL)	Frame Frequency, Power save mode setting
4	IC operation set (ICSET)	LCD drive mode,software reset, display on/off
5	All pixel Control(APCTL)	All pixel control during display ON

■ DETAILED COMMAND DESCRIPTION

D7 (MSB) is bit for command or data judgement
Refer to Command and data transfer method.
C: 0—Next byte is RAM write data
1---Next byte is command

Address set (ADSET)

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
C	0	P5	P4	P3	P2	P1	P0

Address data is specified in P[5:0]
The address range can be set as 000000~100010
When the specified address is out of range, the address will be set to “000000”.
The Reset initialize condition of the DDRAM address is “000000”

Command Register Addresses(read mode):
P[5:0]=23h-----REG1 Register address for software reset condition and EVR setting
P[5:0]=24h-----REG2 Register address for the other settings

EVR Set (EVRSET)

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
C	1	0	P4	P3	P2	P1	P0

It is able to control 32-step electrical register (EVR).
It is able to set V0 voltage level (the max level voltage of LCD driving voltage).

Electrical volume resister (EVR) is set “00000” in reset initialize condition
In “00000” condition, V0 voltage output V_{LCD} voltage.
It is prohibited to set EVR V0 voltage under 2.5V.

■ DETAILED COMMAND DESCRIPTION (Cont.)

The relationship of electrical volume register(EVR) setting and V0 voltage

EVR	Calculation formula	V_{LCD}=5.5V	V_{LCD}=5V	V_{LCD}=4V	V_{LCD}=3.5V	V_{LCD}=3V	V_{LCD}=2.5V
0	V_{LCD}	V0=5.5	V0=5.0	V0=4.0	V0=3.5	V0=3.0	V0=2.5
1	0.967×V_{LCD}	V0=5.323	V0=4.839	V0=3.871	V0=3.387	V0=2.903	V0=2.419
2	0.937×V_{LCD}	V0=5.156	V0=4.688	V0=3.750	V0=3.281	V0=2.813	V0=2.344
3	0.909×V_{LCD}	V0=5.0	V0=4.545	V0=3.636	V0=3.182	V0=2.727	V0=2.273
4	0.882×V_{LCD}	V0=4.853	V0=4.412	V0=3.529	V0=3.088	V0=2.647	V0=2.206
5	0.857×V_{LCD}	V0=4.714	V0=4.286	V0=3.429	V0=3.0	V0=2.571	V0=2.143
6	0.833×V_{LCD}	V0=4.583	V0=4.167	V0=3.333	V0=2.917	V0=2.5	V0=2.083
7	0.810×V_{LCD}	V0=4.459	V0=4.054	V0=3.243	V0=2.838	V0=2.432	V0=2.027
8	0.789×V_{LCD}	V0=4.342	V0=3.947	V0=3.158	V0=2.763	V0=2.368	V0=1.974
9	0.769×V_{LCD}	V0=4.231	V0=3.846	V0=3.077	V0=2.692	V0=2.308	V0=1.923
10	0.750×V_{LCD}	V0=4.125	V0=3.75	V0=3.0	V0=2.625	V0=2.25	V0=1.875
11	0.731×V_{LCD}	V0=4.024	V0=3.659	V0=2.927	V0=2.561	V0=1.195	V0=1.829
12	0.714×V_{LCD}	V0=3.929	V0=3.571	V0=2.857	V0=2.5	V0=2.143	V0=1.786
13	0.697×V_{LCD}	V0=3.837	V0=3.388	V0=2.791	V0=2.442	V0=2.093	V0=1.744
14	0.681×V_{LCD}	V0=3.75	V0=3.409	V0=2.727	V0=2.386	V0=2.045	V0=1.705
15	0.666×V_{LCD}	V0=3.667	V0=3.333	V0=2.667	V0=2.333	V0=2.000	V0=1.667
16	0.652×V_{LCD}	V0=3.587	V0=3.261	V0=2.609	V0=2.283	V0=1.957	V0=1.63
17	0.638×V_{LCD}	V0=3.511	V0=3.191	V0=2.553	V0=2.234	V0=1.915	V0=1.596
18	0.625×V_{LCD}	V0=3.438	V0=3.125	V0=2.5	V0=2.188	V0=1.875	V0=1.563
19	0.612×V_{LCD}	V0=3.367	V0=3.061	V0=2.449	V0=2.143	V0=1.837	V0=1.531
20	0.6×V_{LCD}	V0=3.3	V0=3.0	V0=2.40	V0=2.10	V0=1.8	V0=1.5
21	0.588×V_{LCD}	V0=3.235	V0=2.941	V0=2.353	V0=2.059	V0=1.765	V0=1.471
22	0.576×V_{LCD}	V0=3.173	V0=2.885	V0=2.308	V0=2.019	V0=1.731	V0=1.442
23	0.566×V_{LCD}	V0=3.113	V0=2.83	V0=2.264	V0=1.981	V0=1.698	V0=1.415
24	0.555×V_{LCD}	V0=3.056	V0=2.778	V0=2.222	V0=1.944	V0=1.667	V0=1.389
25	0.545×V_{LCD}	V0=3.0	V0=2.727	V0=2.182	V0=1.909	V0=1.636	V0=1.364
26	0.535×V_{LCD}	V0=2.946	V0=2.679	V0=2.143	V0=1.875	V0=1.636	V0=1.339
27	0.526×V_{LCD}	V0=2.895	V0=2.632	V0=2.105	V0=1.842	V0=1.607	V0=1.316
28	0.517×V_{LCD}	V0=2.845	V0=2.586	V0=2.069	V0=1.810	V0=1.579	V0=1.293
29	0.508×V_{LCD}	V0=2.797	V0=2.542	V0=2.034	V0=1.78	V0=1.525	V0=1.271
30	0.50×V_{LCD}	V0=2.75	V0=2.5	V0=2.0	V0=1.75	V0=1.50	V0=1.250
31	0.491×V_{LCD}	V0=2.705	V0=2.459	V0=1.967	V0=1.72	V0=1.475	V0=1.230

* Incase EVR using, please satisfy V_{LCD}-V0>0.6V.
* If do not satisfy this condition, IC output will be unstable, Do not use V0<2.5V area.

■ DETAILED COMMAND DESCRIPTION (Cont.)

Display control (DISCTL)

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
C	1	1	0	P3	P2	P1	P0

Set Power mode FR

Power save mode FR	P3	P2	Reset initialize condition
Normal mode (80Hz)	0	0	○
Power save mode1 (71Hz)	0	1	
Power save mode2 (64hz)	1	0	
Power save mode3 (50Hz)	1	1	

*Operation current decrease in
Normal mode > Power save mode1 > Power save mode2 > Power save mode3

Set Power mode SR

Power save mode SR	P1	P0	Reset initialize condition
Power save mode1	0	0	
Power save mode2	0	1	
Normal mode	1	0	○
High Power mode	1	1	

*Operation current increase in order of
Power save mode1 < Power save mode2 < Normal mode < High power mode order

Set IC Operation (ICSET)

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
C	1	1	1	0	P2	P1	P0

Set LCD drive waveform

Set up	P2	Reset initialize condition
Line inversion mode	0	○
Frame inversion mode	1	

Operation current: Line inversion > Frame inversion

Set Software Reset condition

Set up	P1	Reset initialize condition
No operation	0	○
Software reset	1	

When “Software Reset” is executed, this device is reset to initial condition.
Software reset is asserted only once when P1 is set. Other settings can be set after this.

■ DETAILED COMMAND DESCRIPTION (Cont.)

Set Display ON and OFF

Set up	P1	Reset initialize condition
Display OFF	0	○
Display ON	1	

Display OFF: the DDRAM content is not affected. All Segment and Common output stop after a frame.
Display OFF mode ends when Display ON is set.
Display ON : SEGMENT and COMMON outputs are active
Start read operation to display data from the DDRAM.

All Pixel control (APCTL)

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
C	1	1	1	1	0	P1	P0

All display set ON

Set up	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

All display off

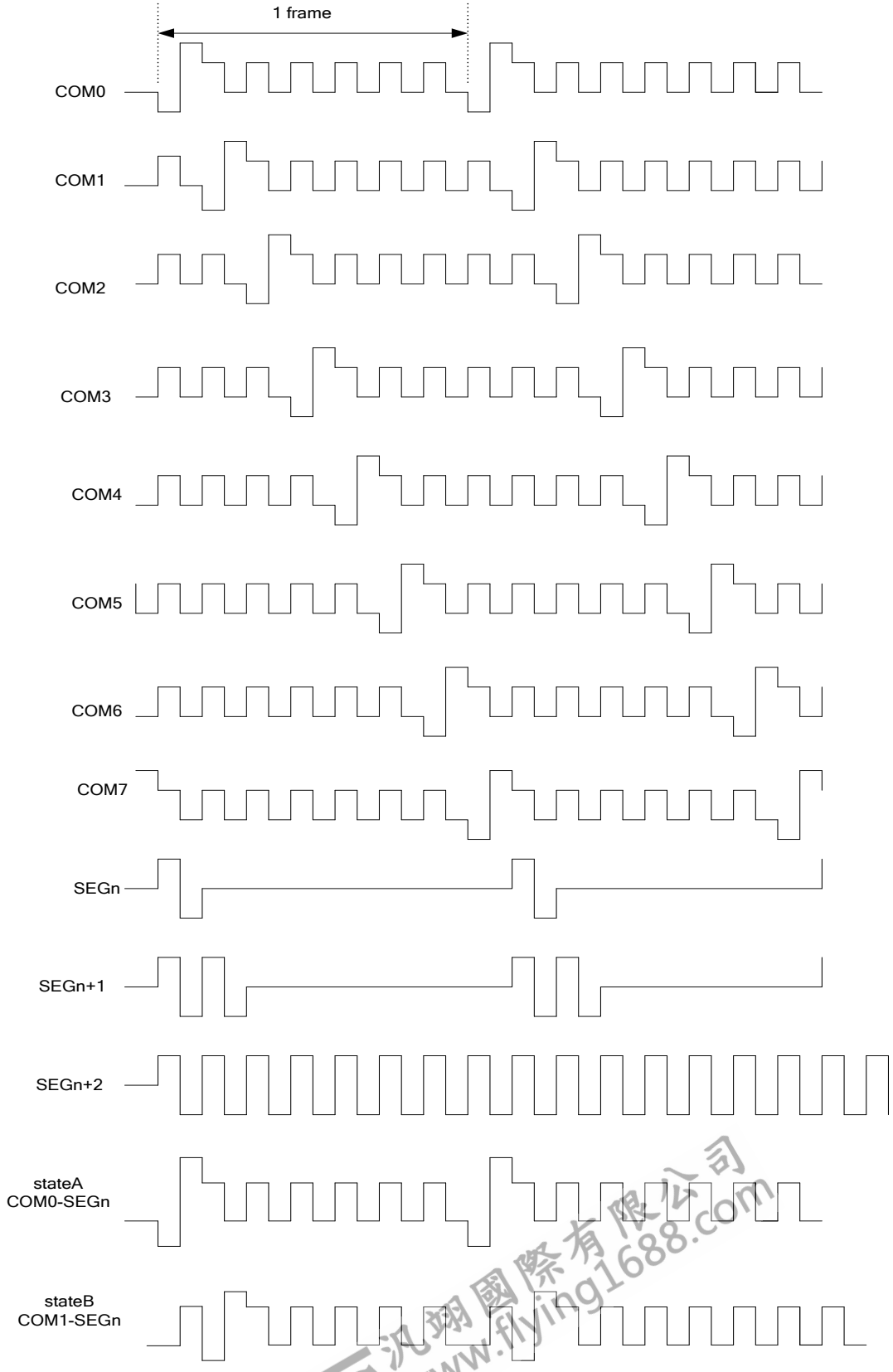
Set up	P1	Reset initialize condition
Normal	0	○
All pixel OFF	1	

All pixels ON : All pixels are ON regardless of DDRAM data
All pixels OFF : All pixels are OFF regardless of DDRAM.

Note: All pixels ON/OFF is effective only at the time of “Display ON” status.
The contents of DDRAM do not change at this time.
When P1 and P0=’1’, APOFF is selected. APOFF has higher priority than APON.

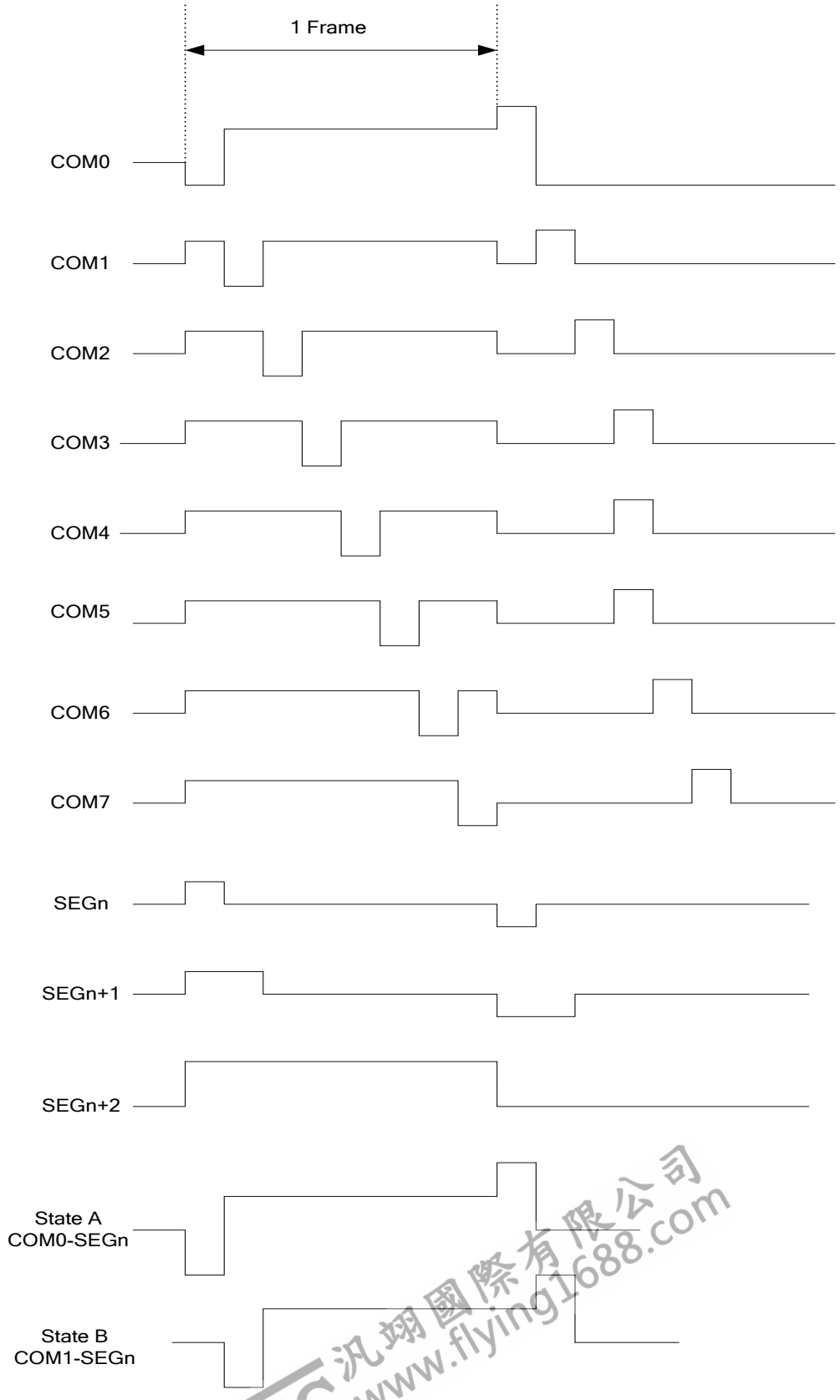
■ LCD DRIVING WAVEFORM

Line inversion mode (1/4 bias, 1/8 duty)



■ LCD DRIVING WAVEFORM (Cont.)

Frame inversion mode



■ TYPICAL APPLICATION CIRCUIT